

COMPAL CONFIDENTIAL

MODEL NAME : VAW30
PCB NO : LA-9832P (DA8000XL000)
BOM P/N : 4319M931L01
GPIO MAP: X.X

Alpine 14"

Haswell ULT


2013-08-23(Gerber)
REV : 1.0

- @ : Nopop Component
- 1@ : M/B SPI ROM
- TAA@ : TAA/B SPI ROM
- CONN@ : Connector Component
- DIS@ : Discrete Pop Component
- UMA@ : UMA Pop Component
- EMI@ : EMI Component
- ESD@ : ESD Component
- RF@ : RF Component
- XDP@ : XDP Component
- eTP@ : TS eTP Component
- NeTP@ : TS non - eTP Component
- 76_U3@ : USB 3.0 Redriver
- 1 @ 2 : Short_Pad

Interleaved Memory

MB PCB	
Part Number	Description
DAXXXXXXXX	PCB OLD LA-9832P REV1 M/B DIS

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

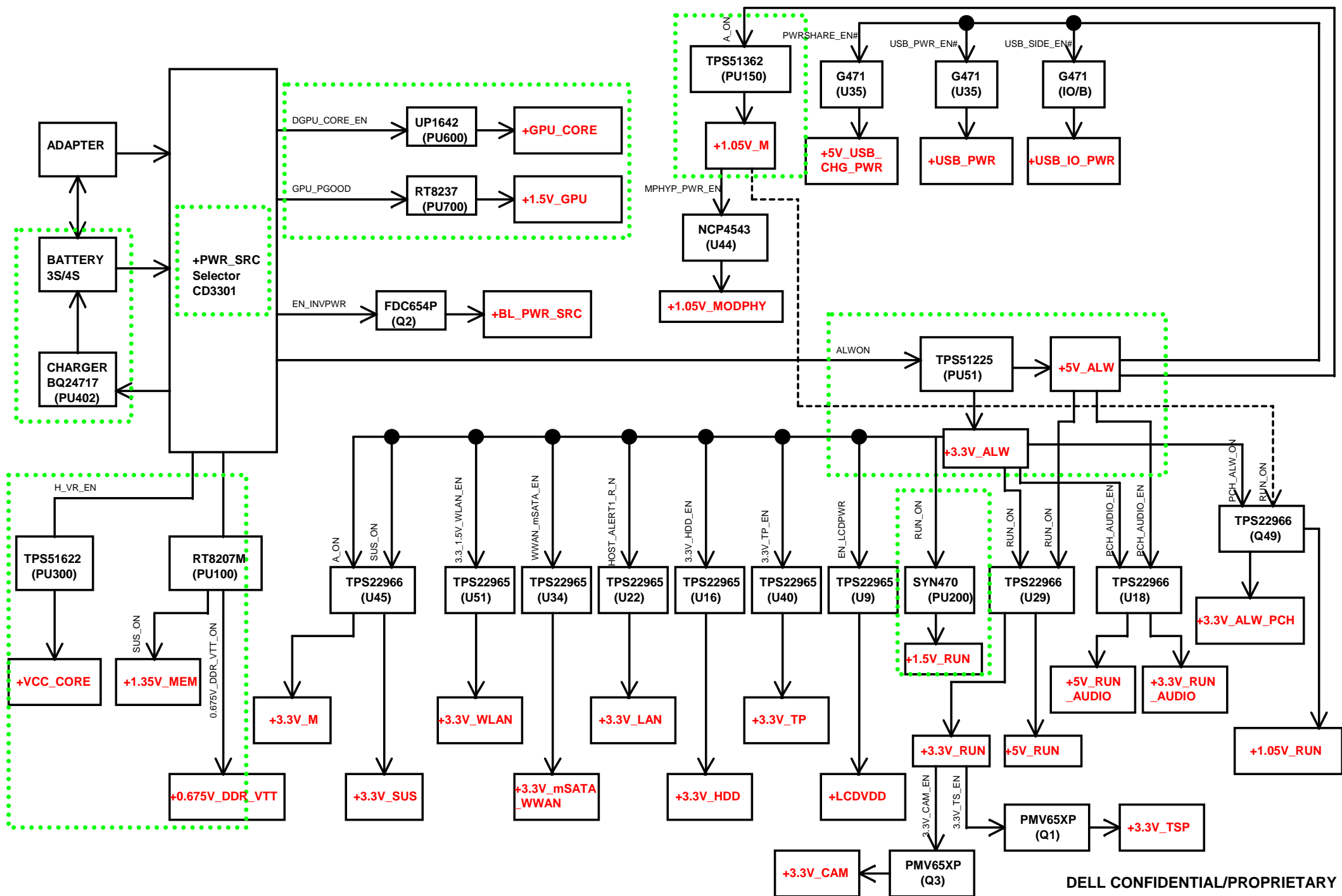
PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->MB-->LEFT
	USB3.0 2		USB3.0-->IOB-->Rear Right
PCIE 1	USB3.0 3		PCIE1-->MMI PCIE
PCIE 2	USB3.0 4		USB3.0-->Docking
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			GPU(DIS)/Express card(UMA)
PCIE 6		SATA 3	WWAN(mSATA)/Express card(PCIE)
		SATA 2	ODD
		SATA 1	HDD
		SATA 0	DOCK

HSW ULT	USB PORT#	DESTINATION
	0	IO (Right)
	1	JUSB1(Left)
	2	USB DB(Rear Left)
	3	DOCK
	4	Dock
	5	WebCAM
	6	Touch Screen
	7	USB HUB

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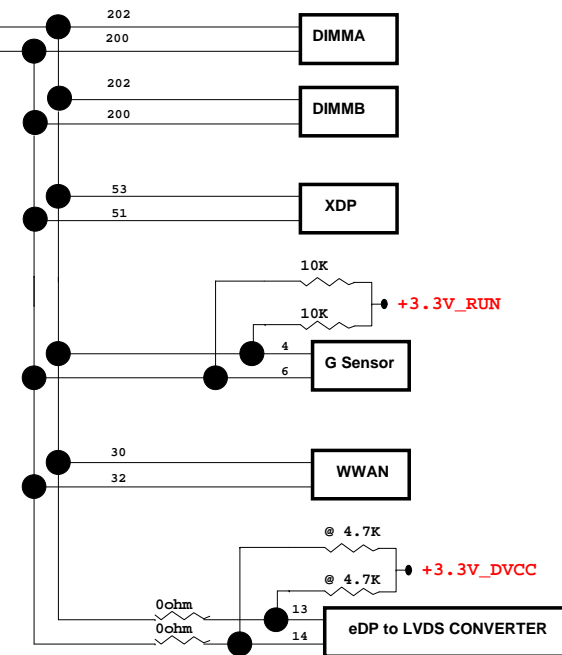
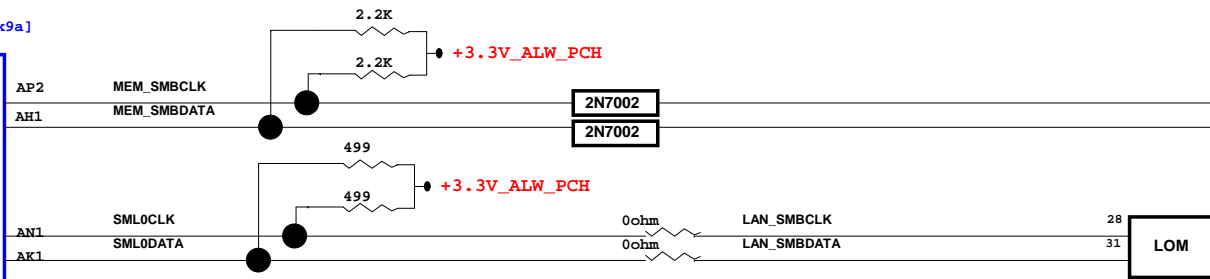
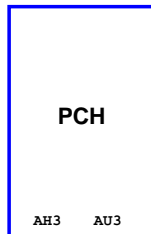


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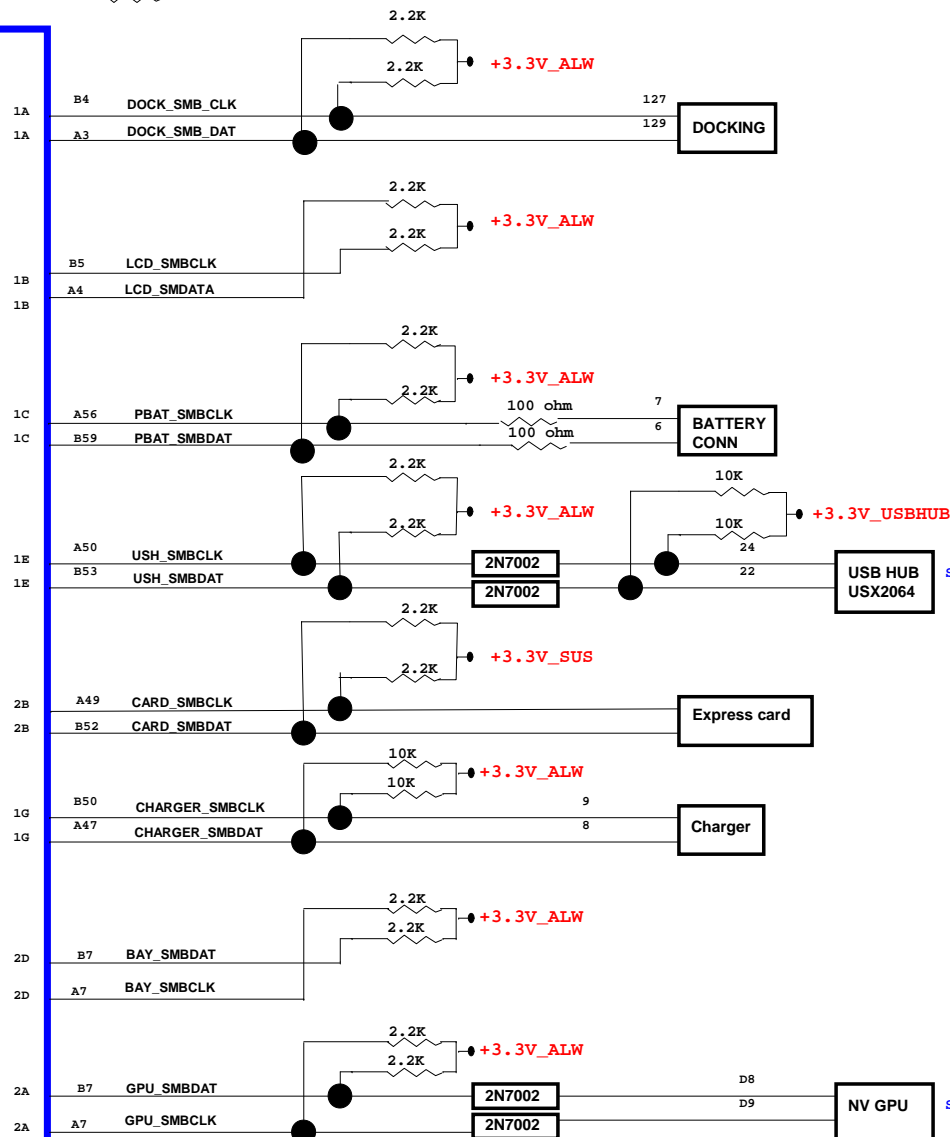
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Power Rail			
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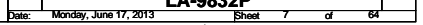
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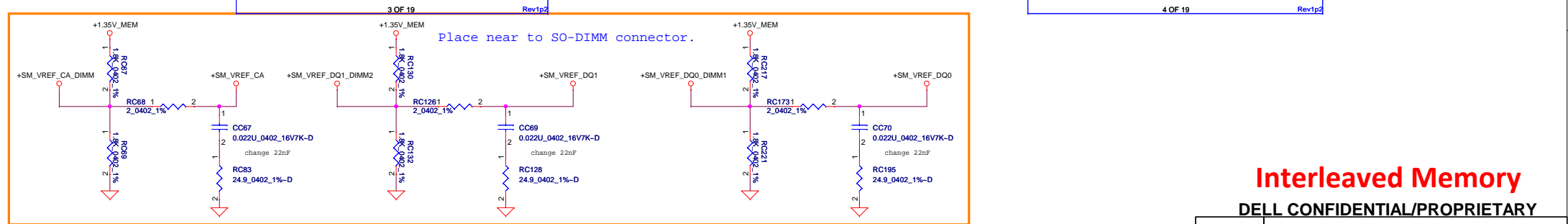
KBC



MEC 5075



DDR interleave routing



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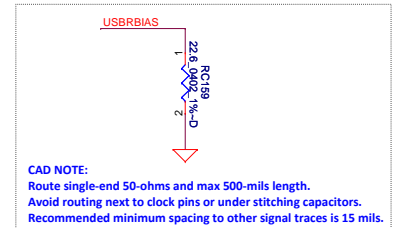
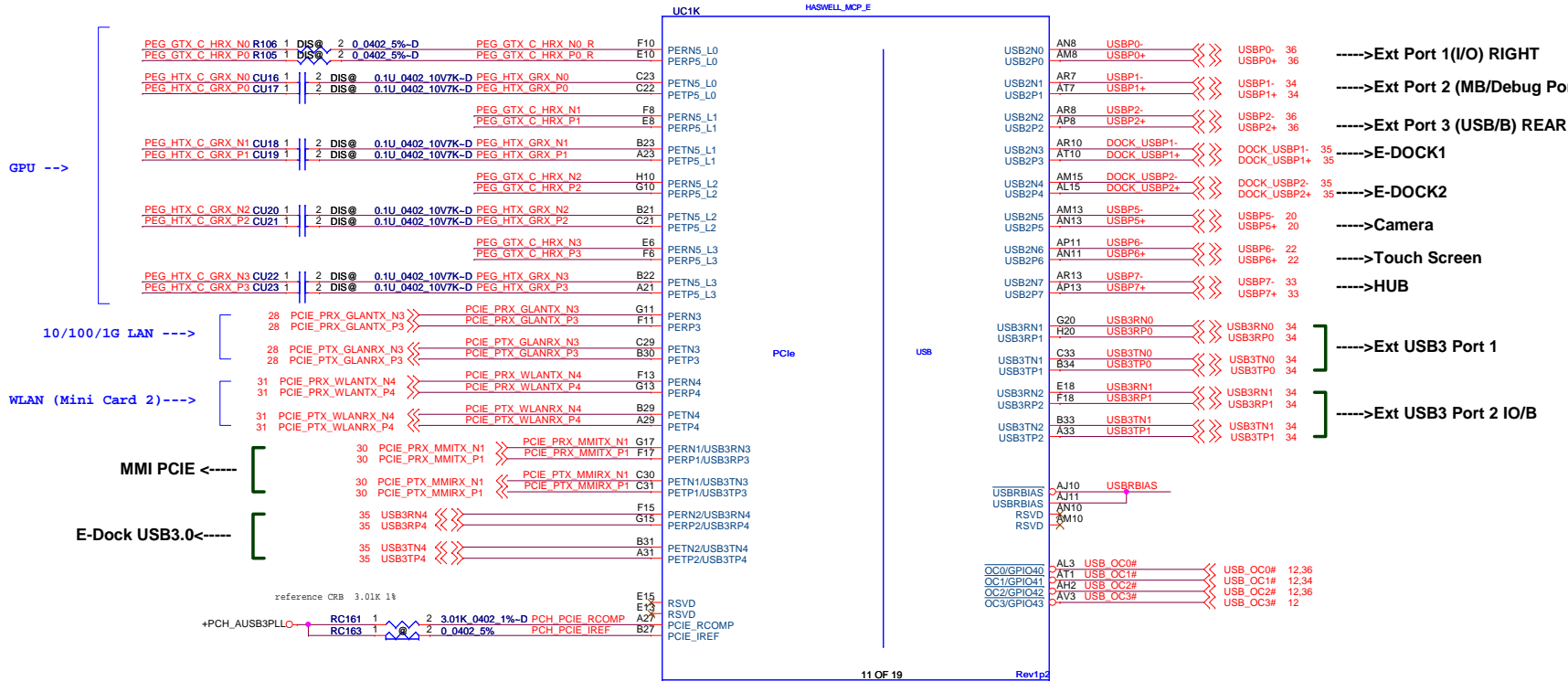
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MCP(3/12) DDR3

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MCP(3/12) DDR3			
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42 PEG_GTX_C_HRX_N[0..3] >> PEG_GTX_C_HRX_N[0..3]
42 PEG_GTX_C_HRX_P[0..3] >> PEG_GTX_C_HRX_P[0..3]
42 PEG_HTX_C_GRX_N[0..3] << PEG_HTX_C_GRX_N[0..3]
42 PEG_HTX_C_GRX_P[0..3] << PEG_HTX_C_GRX_P[0..3]

32 PEG_GTX_C_HRX_N0_M >> PEG_GTX_C_HRX_N0_M R101 1 UMA@ 2 0 0402 5%-D PEG_GTX_C_HRX_N0_R
32 PEG_GTX_C_HRX_P0_M >> PEG_GTX_C_HRX_P0_M R100 1 UMA@ 2 0 0402 5%-D PEG_GTX_C_HRX_P0_R
32 PEG_HTX_C_GRX_N0_M << PEG_HTX_C_GRX_N0_M R102 1 UMA@ 2 0 0402 5%-D PEG_HTX_C_GRX_N0
32 PEG_HTX_C_GRX_P0_M << PEG_HTX_C_GRX_P0_M R104 1 UMA@ 2 0 0402 5%-D PEG_HTX_C_GRX_P0



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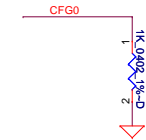
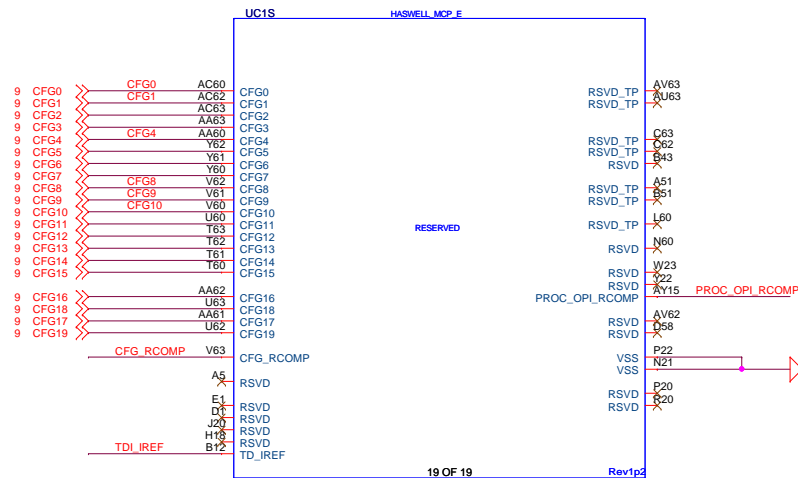
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Title		MCP(6/12) PCIE,USB	
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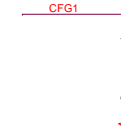
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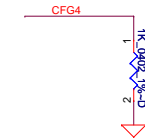
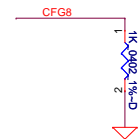
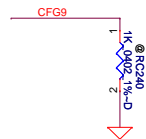
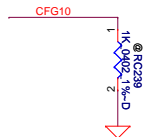
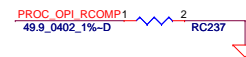
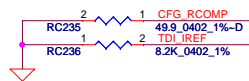
CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed



PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed



SAFE MODE BOOT	
CFG10	<p>1: POWER FEATURES ACTIVATED DURING RESET</p> <p>0: POWER FEATURES (ESPECIALLY CLOCK GATING) ARE NOT ACTIVATED</p>

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	<p>1: VRs support SVID protocol are present</p> <p>0: No VR support SVID is present</p> <p>The chip will not generate (OR Respond to) SVID activity</p>

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	<p>1: Enable(Default): Noa will be disable in locked units and enable in un-locked units</p> <p>0: Enable Noa will be available peggardless of the locking of the unit</p>

Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

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MCP(8/12) CFG, RSVD

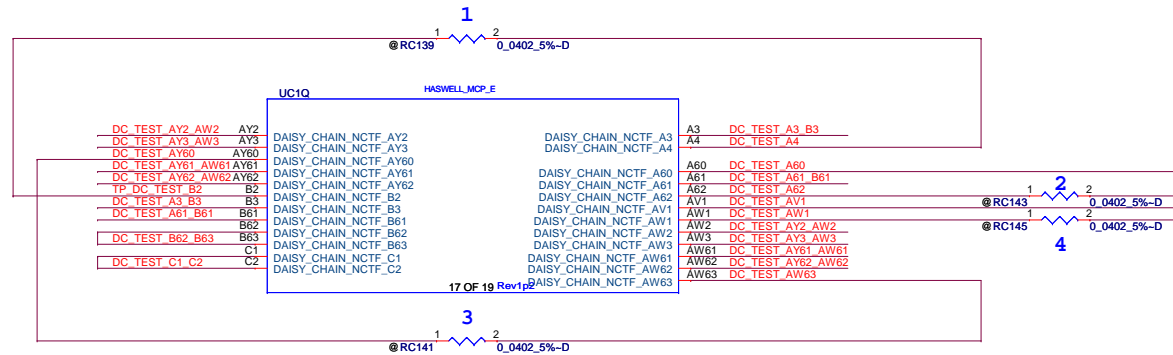
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LA-9052F

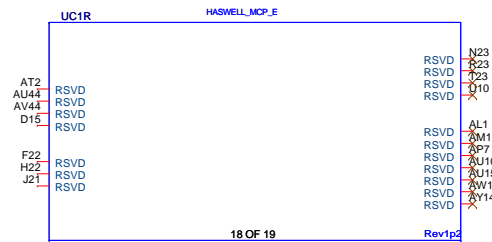
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Package Daisy Chain:

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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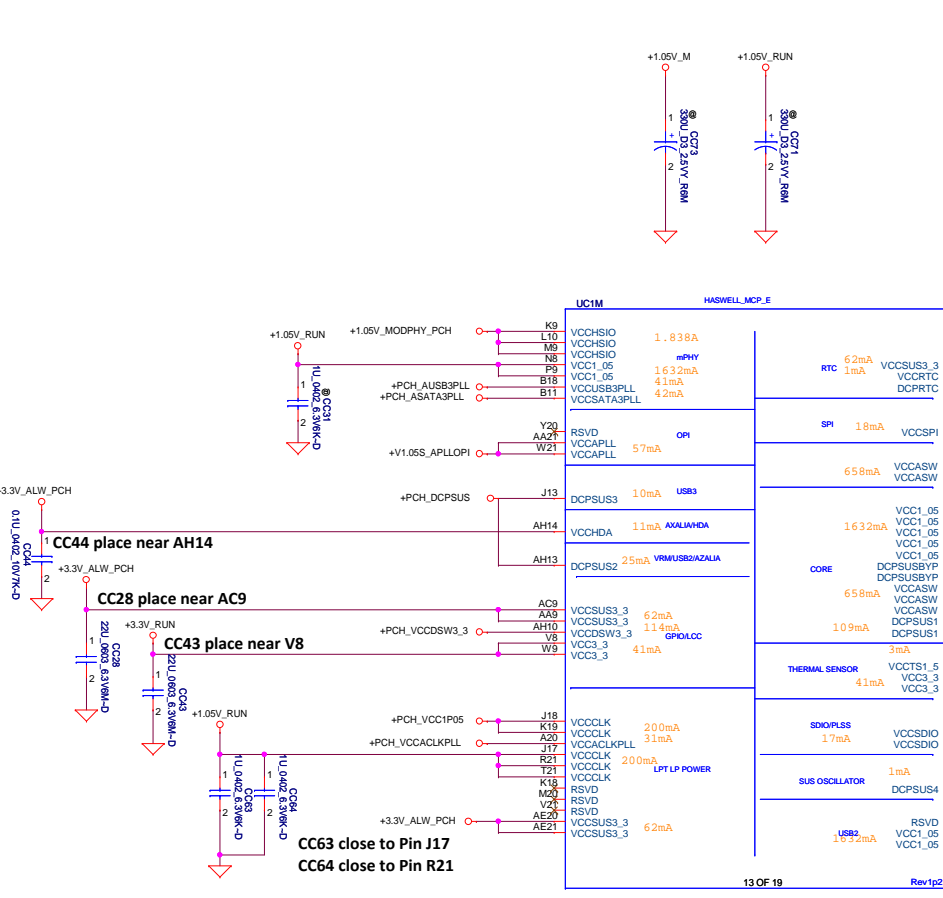
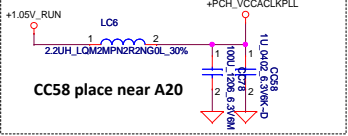
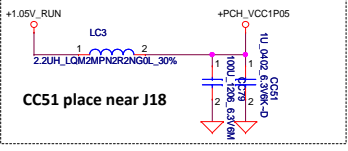
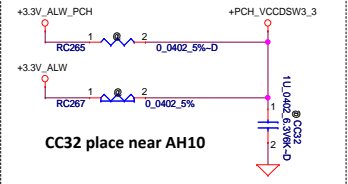
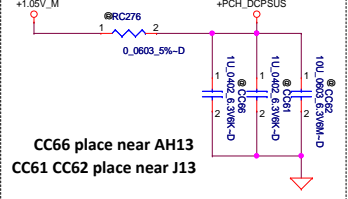
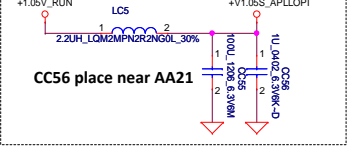
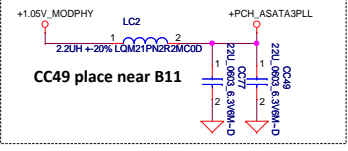
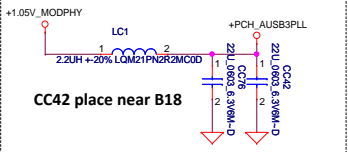
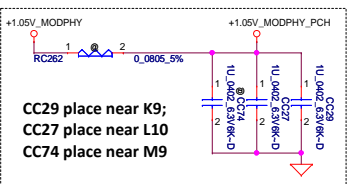
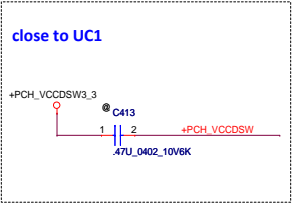
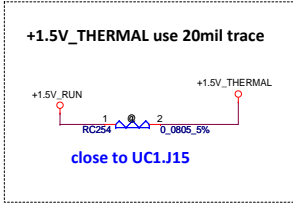


Table 6-3. Pre-Si I_{CC} max Estimates

Voltage Rail	Voltage (V)	S0 Iccmax (A) ¹	Sx Iccmax (A) ²	Deep Sx Iccmax (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCSDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μA See notes 1, 2



DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267

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MCP(11/12) Power

LA-9832P

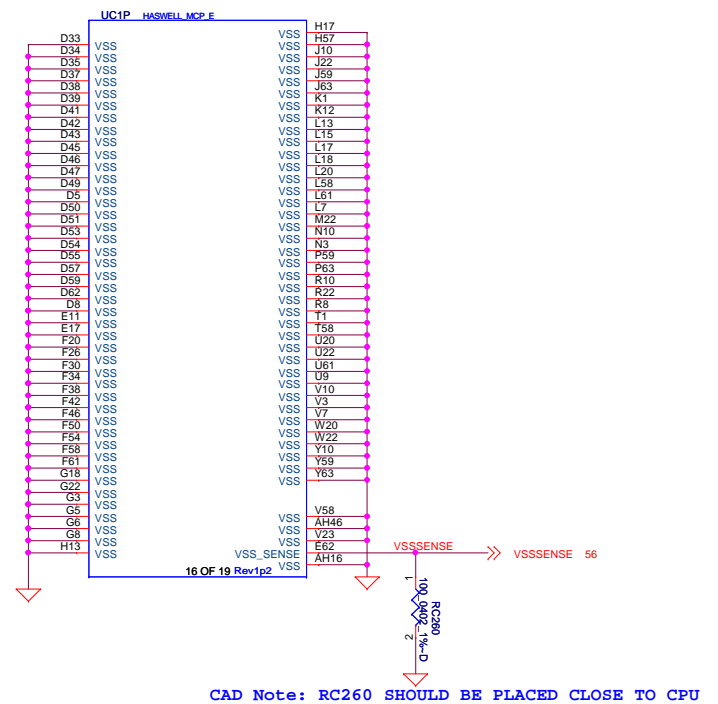
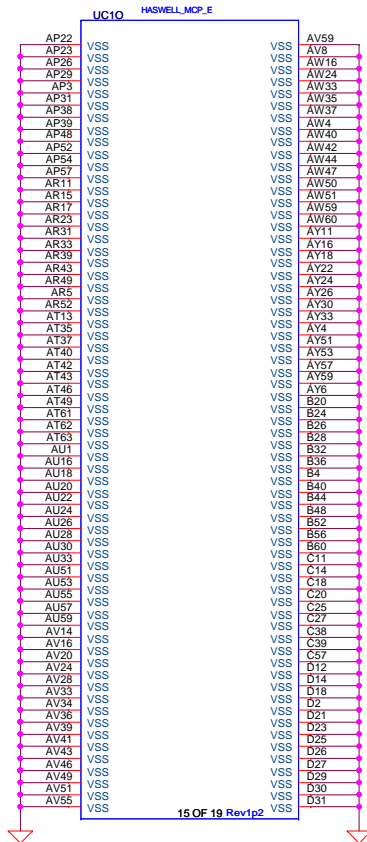
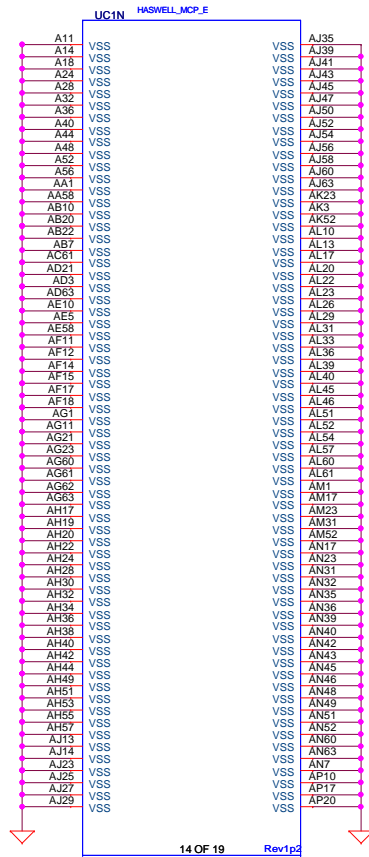
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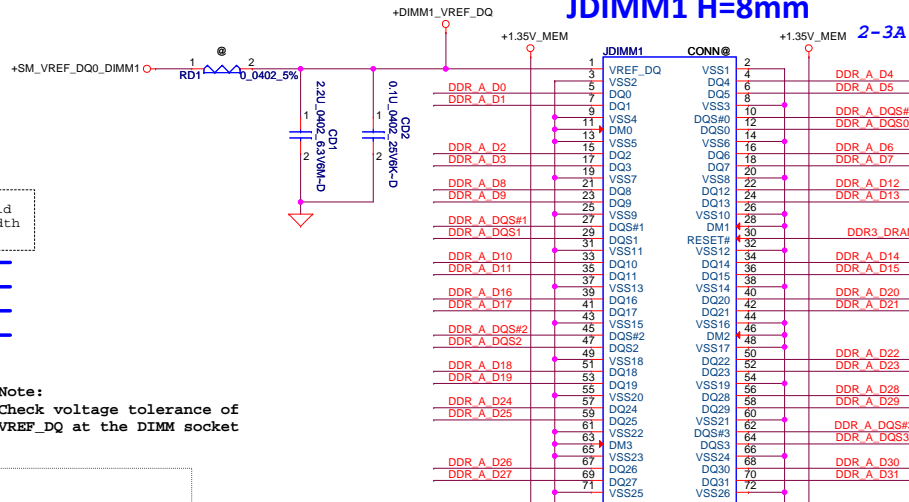


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MCP(12/12) VSS			
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JDIMM1 H=8mm

2-3A to 1 DIMMs/channel

Reverse Type

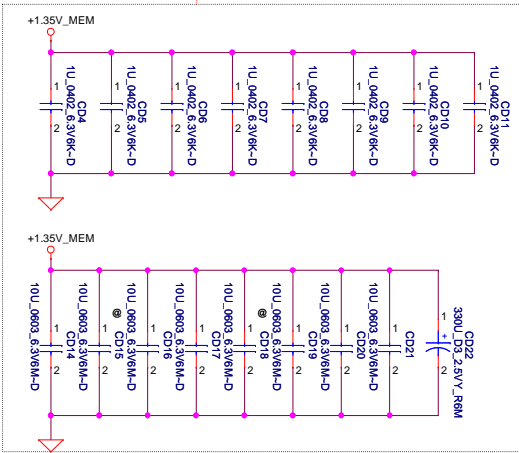


All VREF traces should have 10 mil trace width

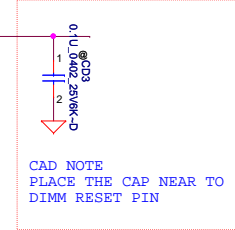
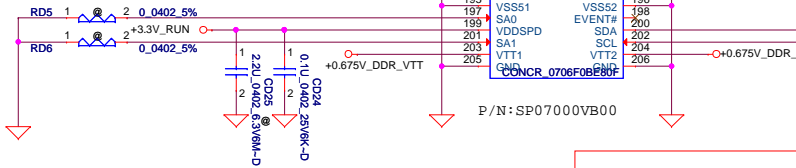
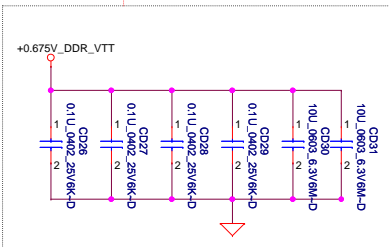
8 DDR_A_DQS#0[.7] <<>>
8 DDR_A_D0[.63] <<>>
8 DDR_A_DQS[0.7] <<>>
8 DDR_A_MA[0.15] <<>>

Layout Note:
Place near JDIMM1

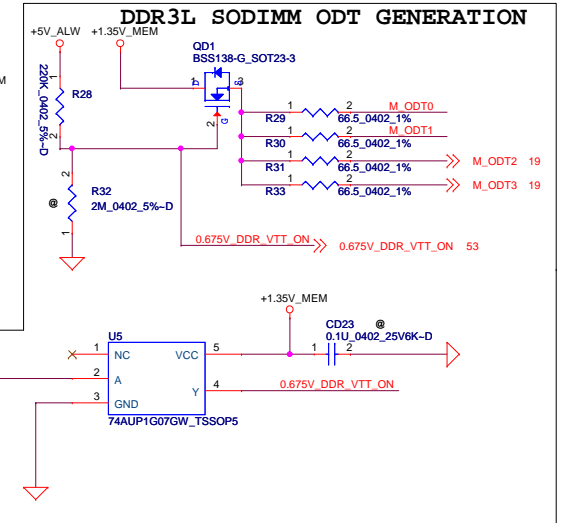
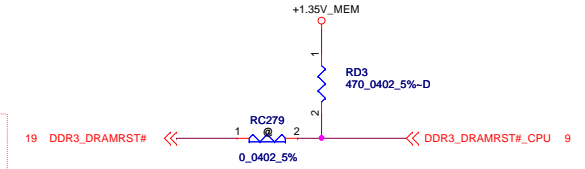
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203,204



CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



Interleaved Memory

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DDRIII DIMM1			
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JDIMM2 H=4mm 2-3A to 1 DIMMs/channel

Reverse Type

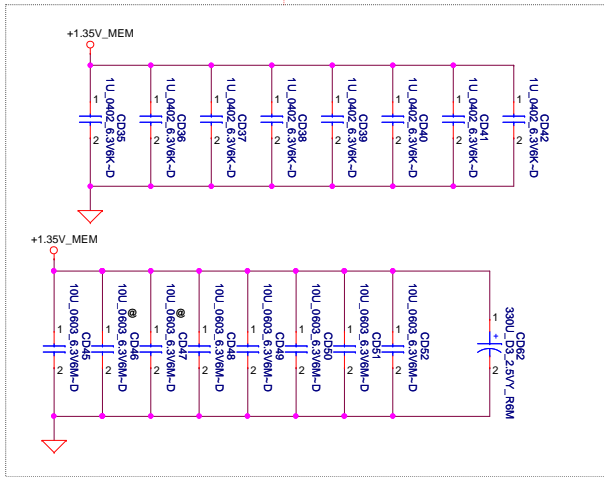
- 8 DDR_B_DQS#[0..7] <<>
- 8 DDR_B_DQ[0..63] <<>
- 8 DDR_B_DQS#[0..7] <<>
- 8 DDR_B_MA[0..15] <<>

All VREF traces should have 10 mil trace width

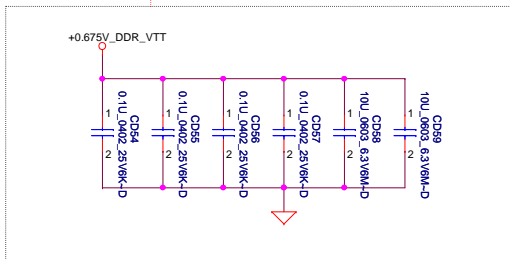
Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



Layout Note:
Place near JDIMM2.203,204



+3.3V_RUN

0.0402 5% RD10

+0.675V_DDR_VTT

0.0402 5% RD11

0.0402 5% RD12

0.0402 5% RD13

0.0402 5% RD14

0.0402 5% RD15

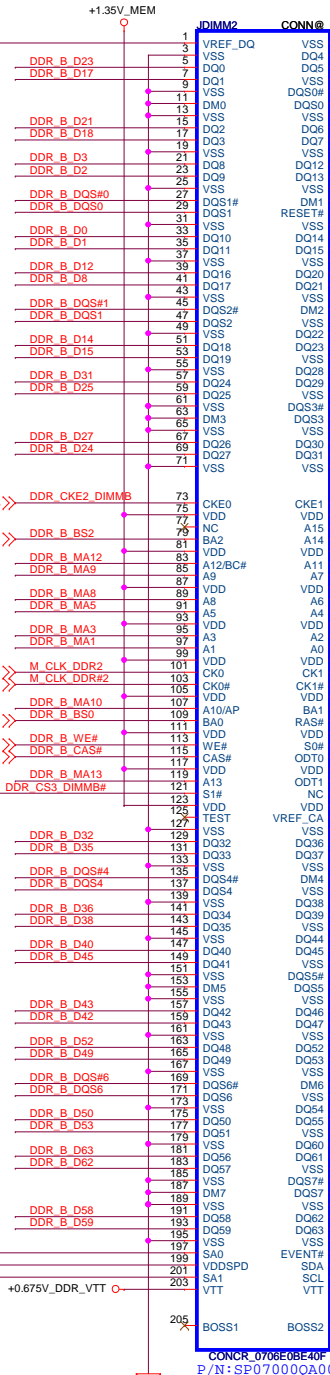
0.0402 5% RD16

0.0402 5% RD17

0.0402 5% RD18

0.0402 5% RD19

0.0402 5% RD20



CONC'R 0706E0B40F
P/N: SP07000QA00

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Interleaved Memory

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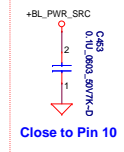
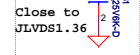
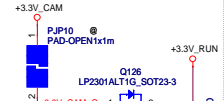
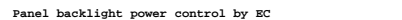
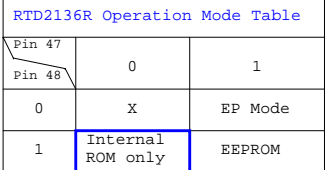
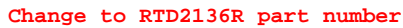
Compal Electronics, Inc.

DDRIII DIMM2

LA-9832P

Rev 0.5

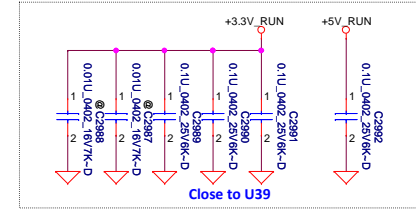
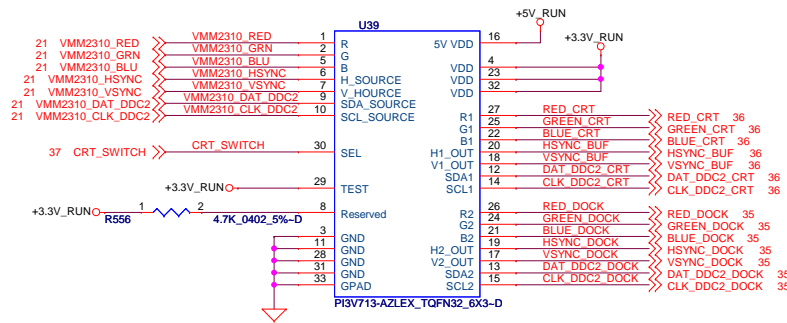
Date: Thursday, June 13, 2013 Sheet 19 of 64



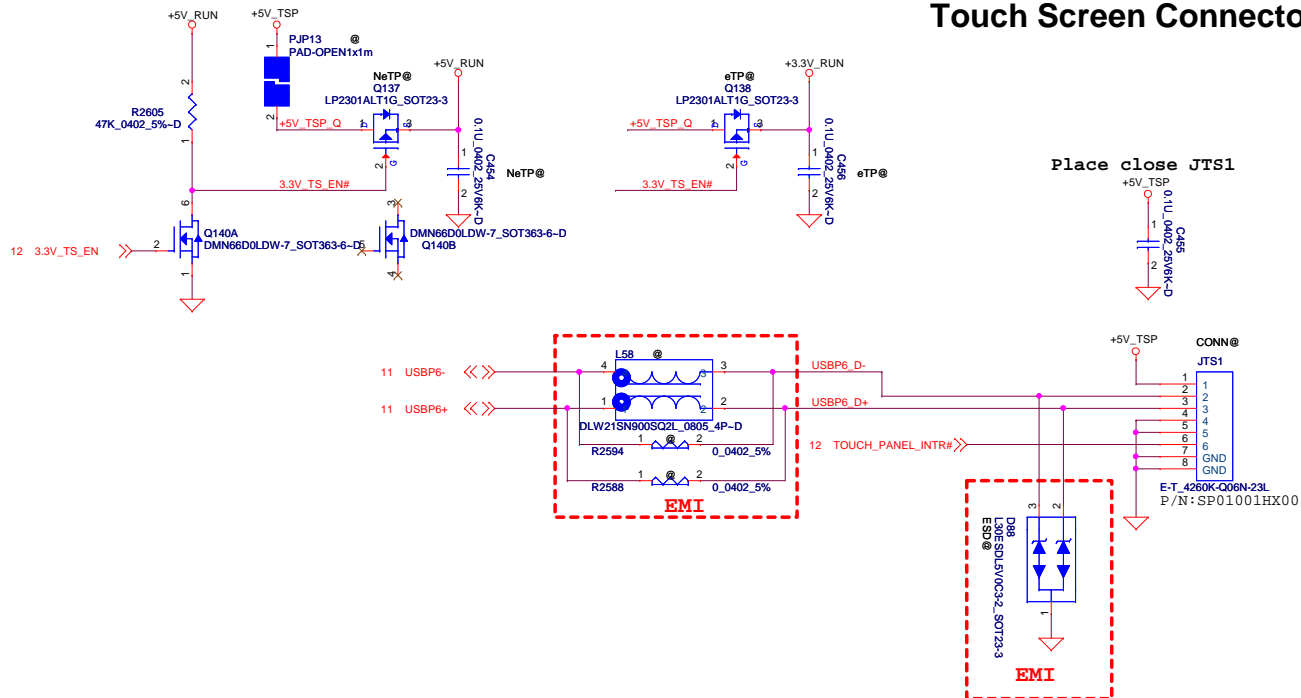
LCD Power

CRT SW for MB/DOCK

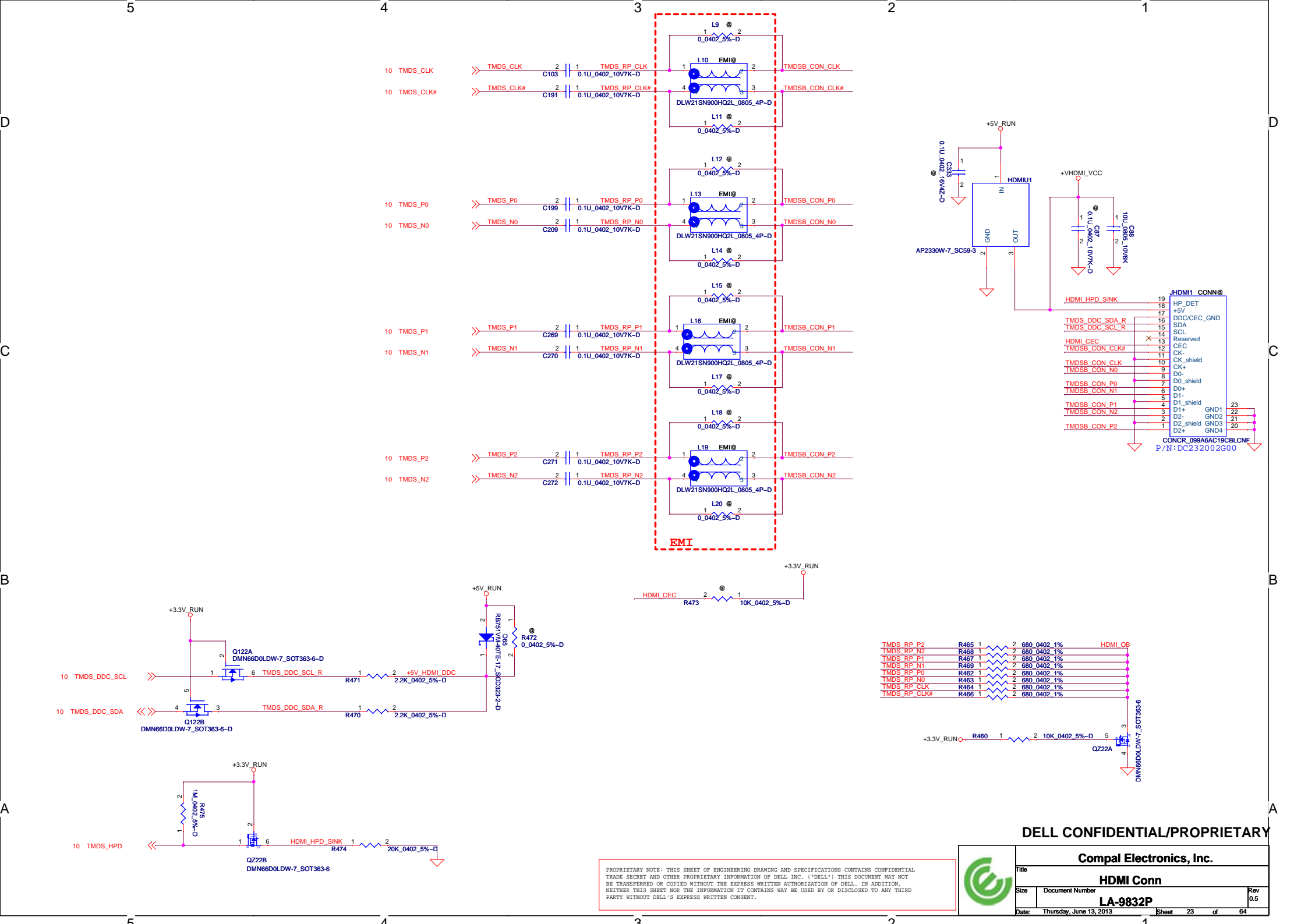
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



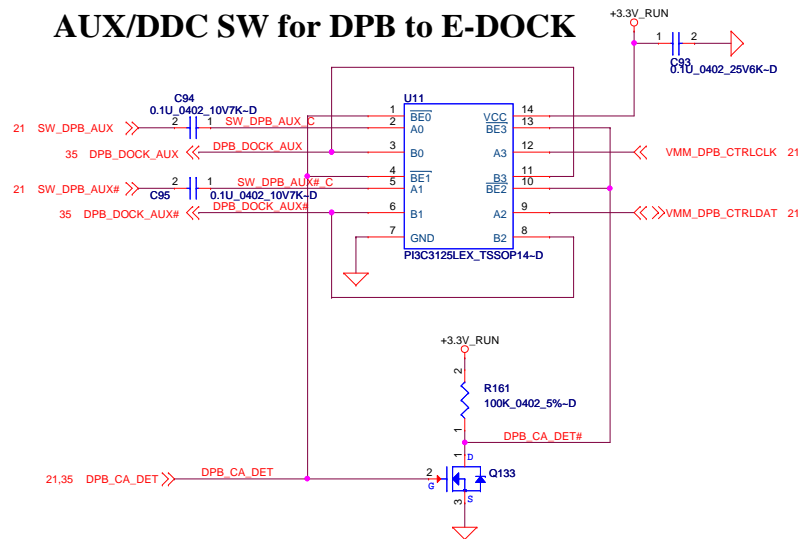
Touch Screen Connector



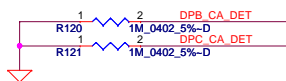
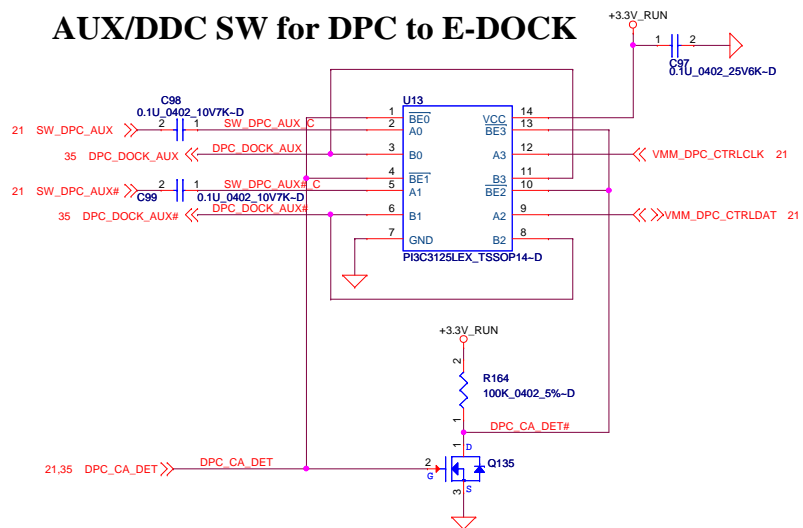
Security Classification	Compal Secret Data	Title	
Issued Date	2011/07/15	Deciphered Date	2012/07/15
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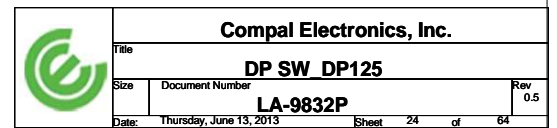
AUX/DDC SW for DPB to E-DOCK



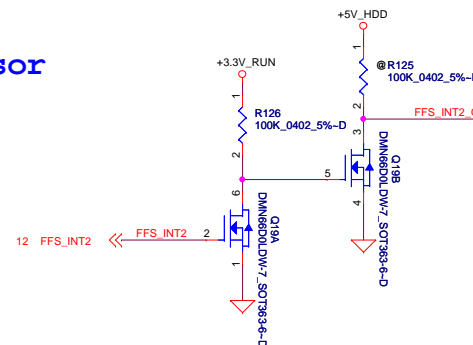
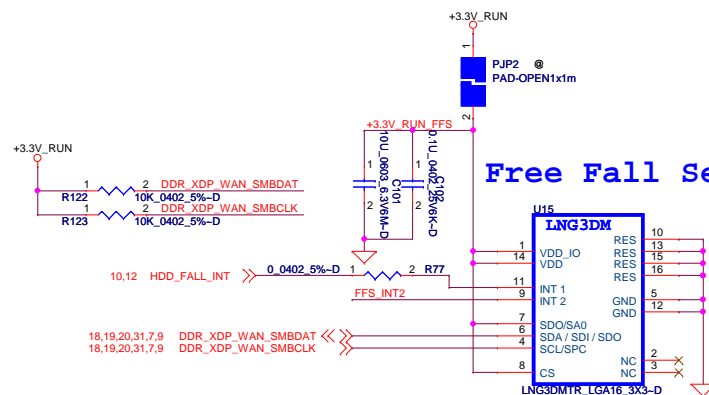
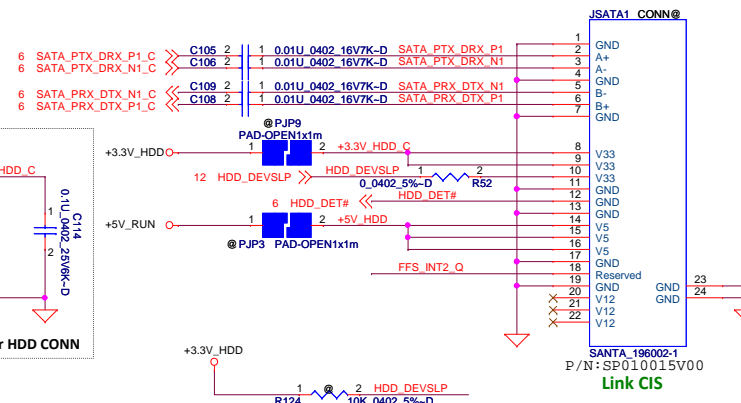
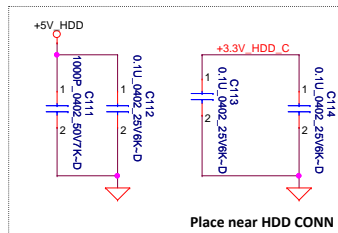
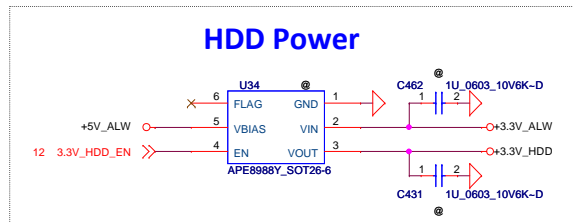
AUX/DDC SW for DPC to E-DOCK



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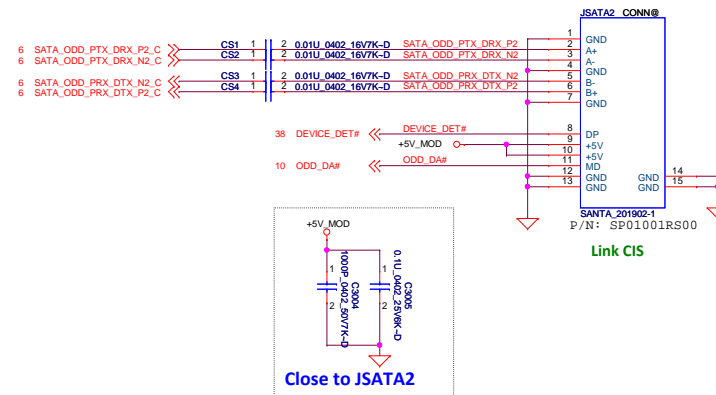
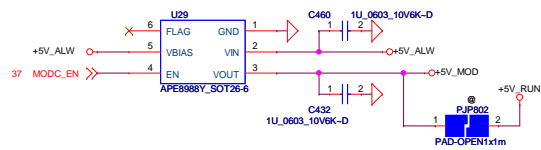
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HDD CONN				Rev
Title	HDD CONN			0.5
Size	Document Number	LA-9832P		
Date	Thursday, June 13, 2013	Sheet	25	of 64

ODD power



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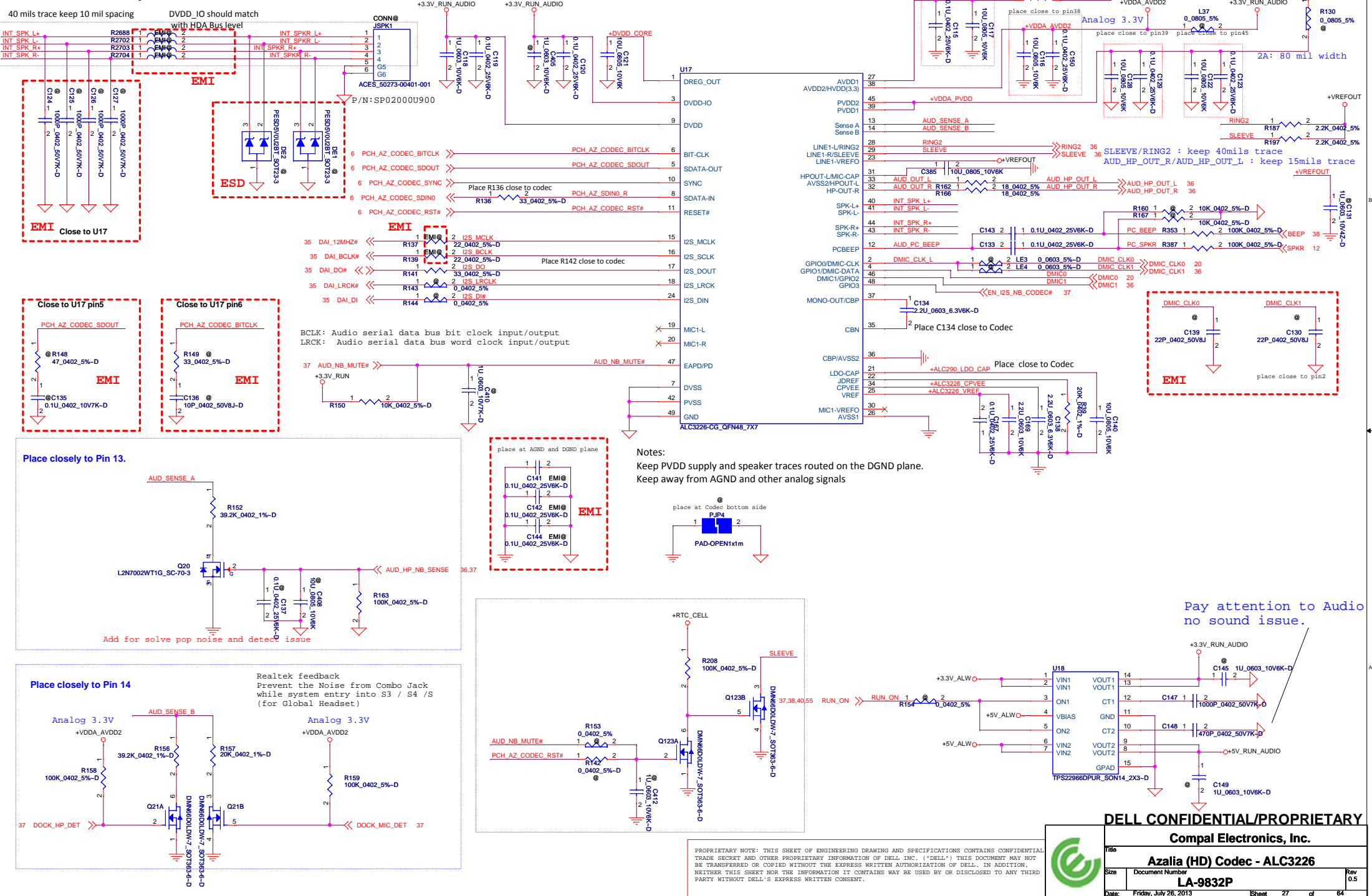


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Size	Document Number	LA-9832P	
Date:	Thursday, June 13, 2013	Sheet	26 of 64

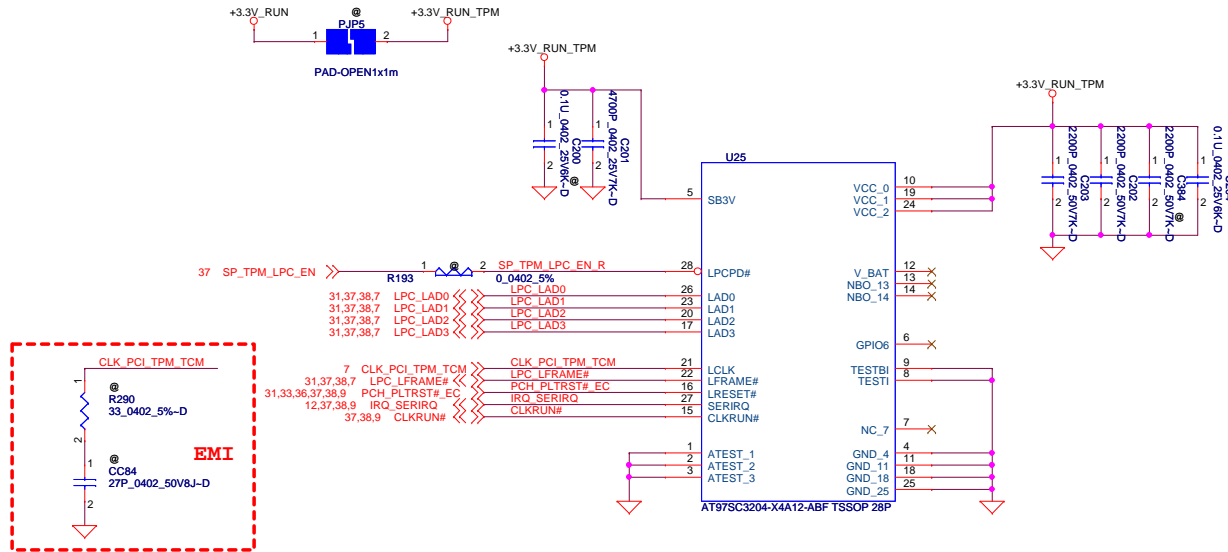
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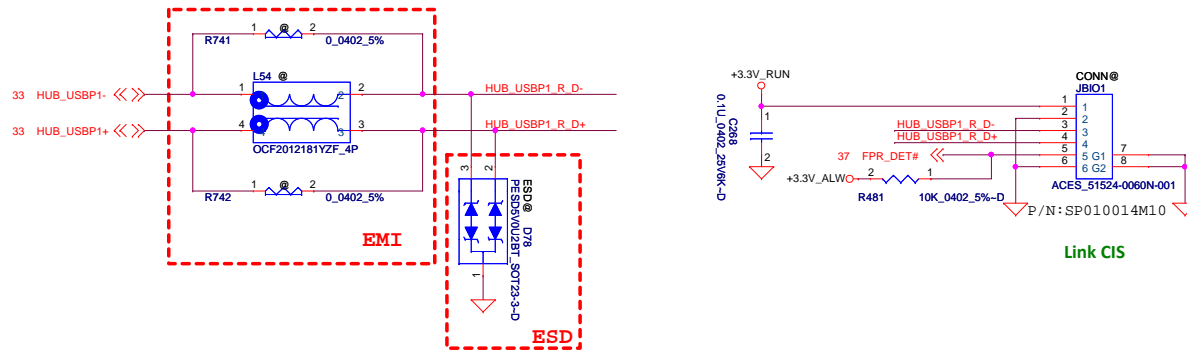
Internal Speakers Header



ATMEL TPM



Finger print module



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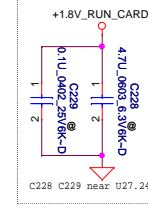
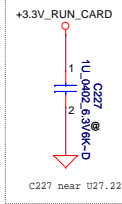
Title			
TPM/FP			
Size	Document Number	Rev	
	LA-9832P	0.5	
Date:	Thursday, June 13, 2013	Sheet	29 of 64

homestay ES1(no SD4.0)

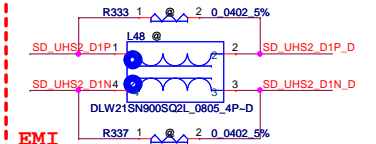
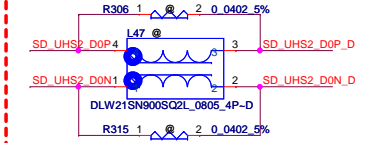
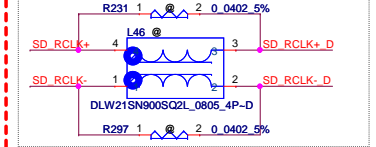
M00 (symbol has been updated 26~36 pin swap)

OZ777FJ2LN

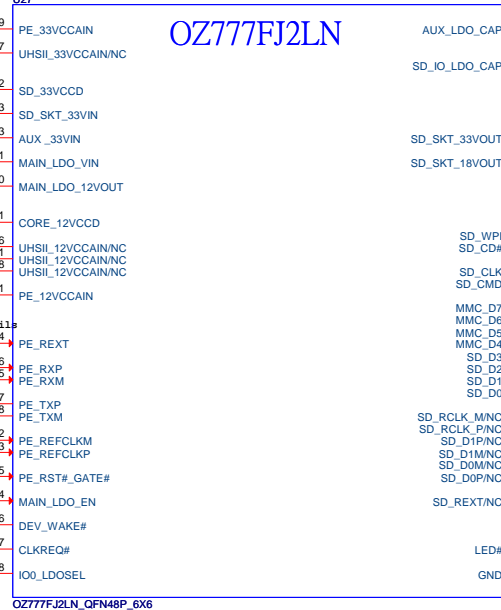
C215 must close to U27.27 within 50mils
C214 must close to U27.9 within 50mils
C213 must close to U27.9 with 100mils
L35 must close to U38.9 within 200mils
+3.3V_RUN_AIN trace width 30mils



please routing daisy chain
1. from U27.38 (SD_D0) -> U27.32 (SD_RCLK_P) -> L46.4
2. From U27.37 (SD_D1) -> U27.33 (SD_RCLK_N) -> L46.1

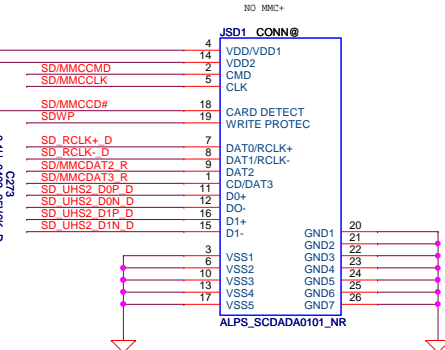
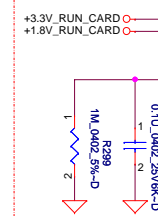
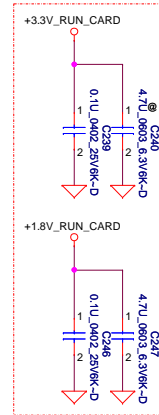


EMI



OZ777FJ2LN_QFN48P_6X6

Near to JSD1



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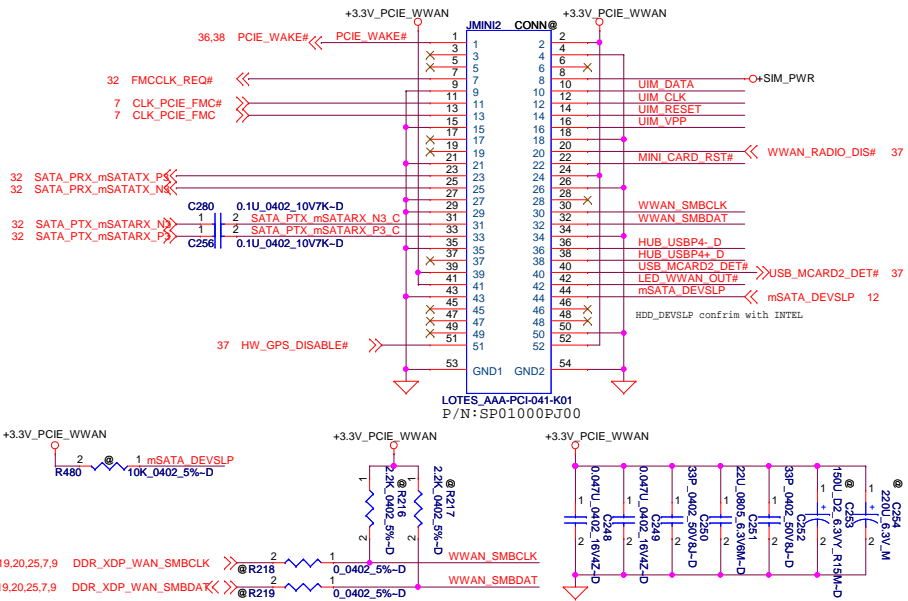
Card Reader OZ777FJ2

LA-9832P

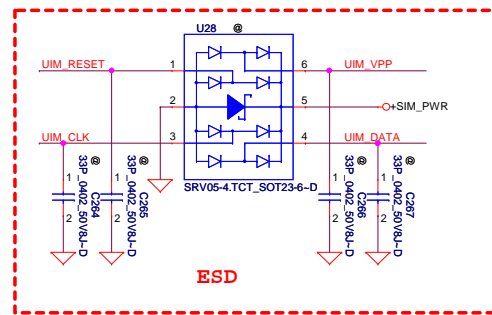
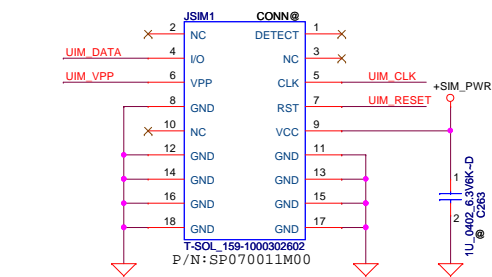
Size	Document Number	Rev
Thursday, June 13, 2013	Sheet 30 of 64	0.5

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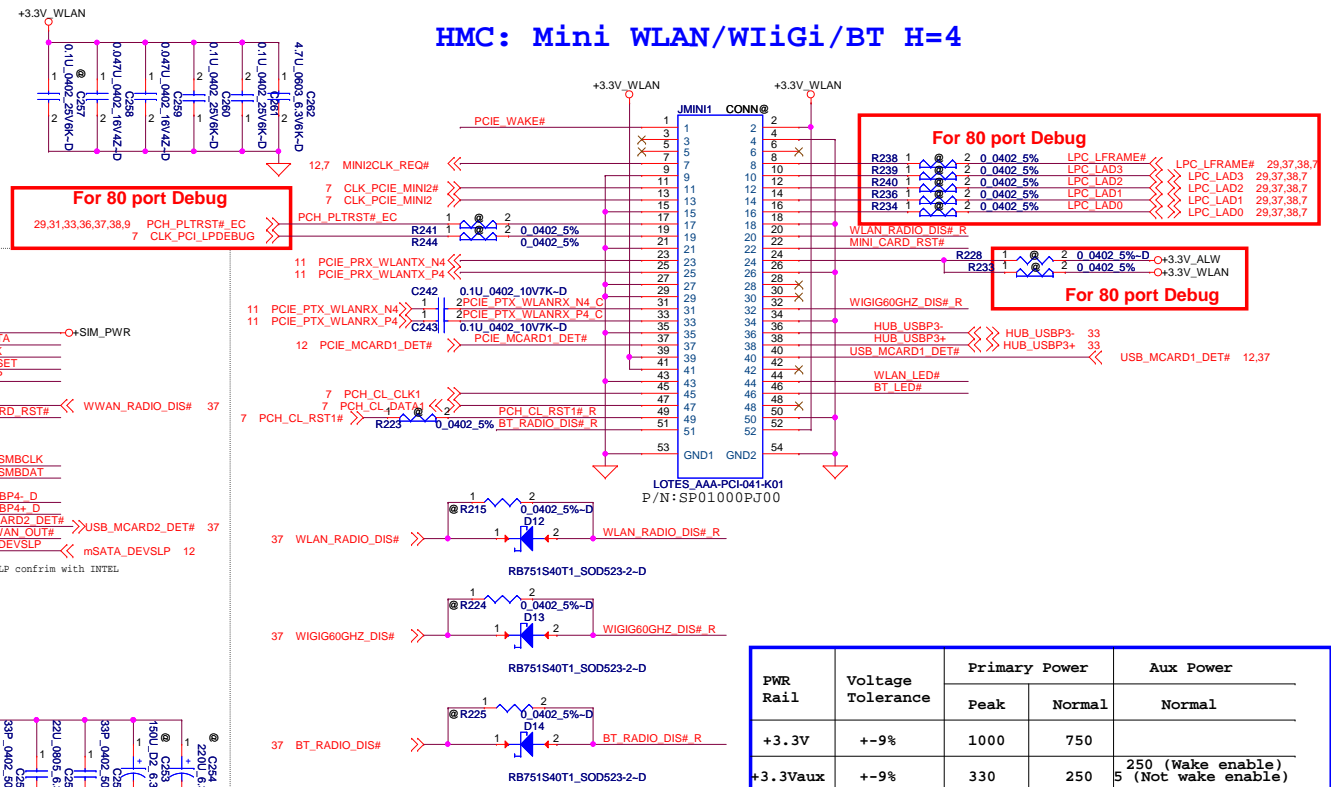
FMC: Mini WWAN/LTE H=8



uSIM Card Push-Push

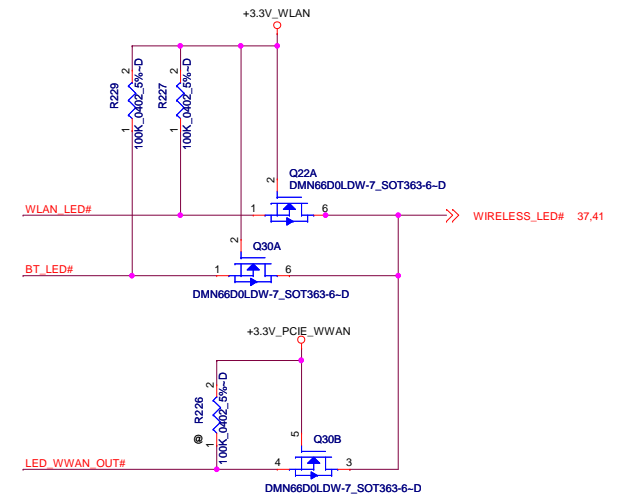
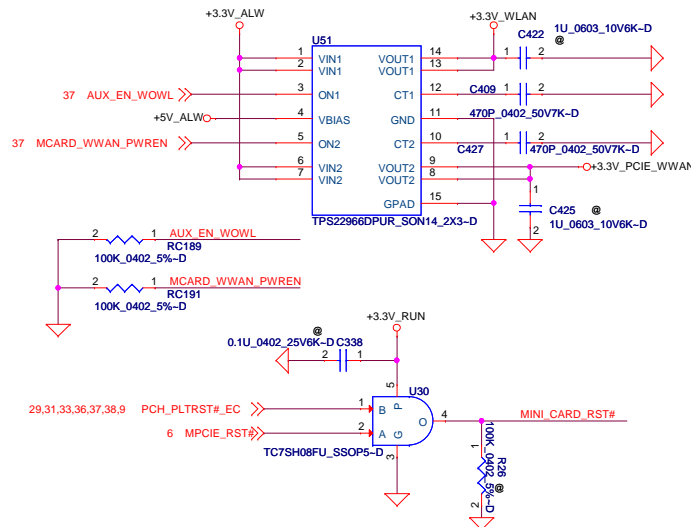


HMC: Mini WLAN/WiGi/BT H=4



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)

LED control circuit



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Mini Card/SIM Card

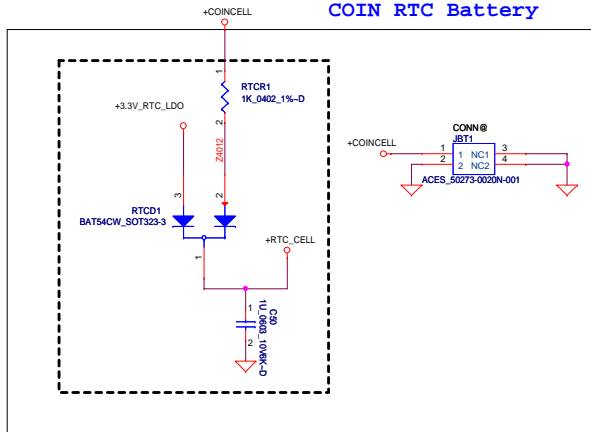
LA-9832P

0.5

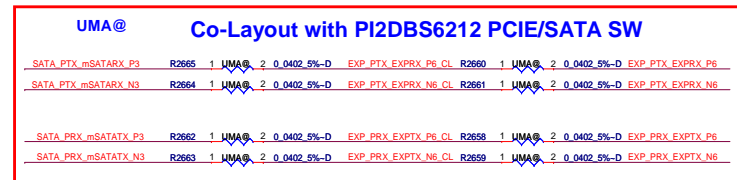
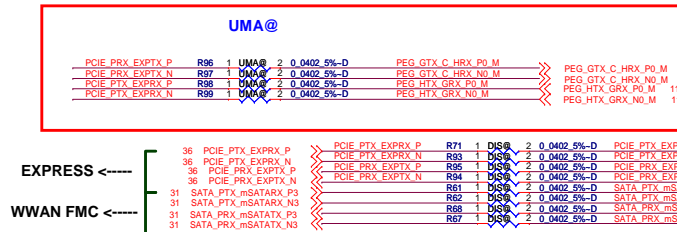
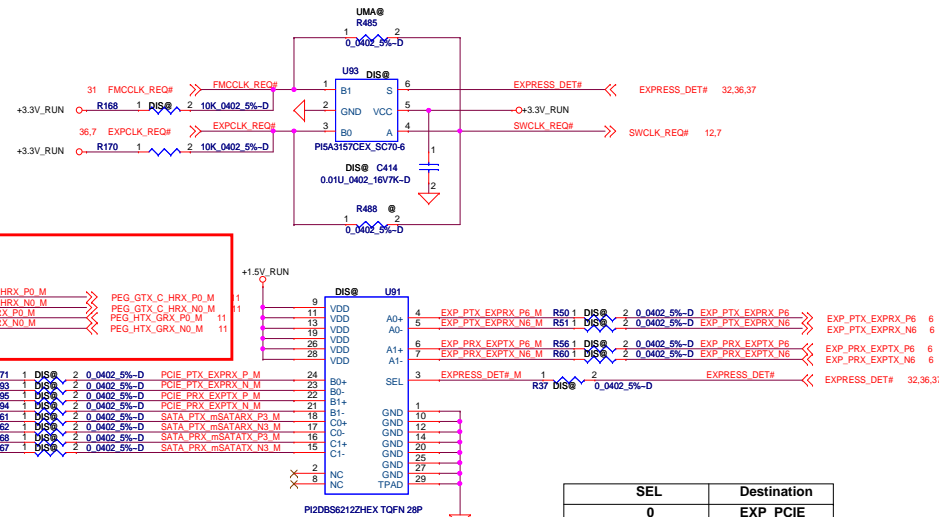
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EXP/FMC PCIe clock/REQ Switch

COIN RTC Battery



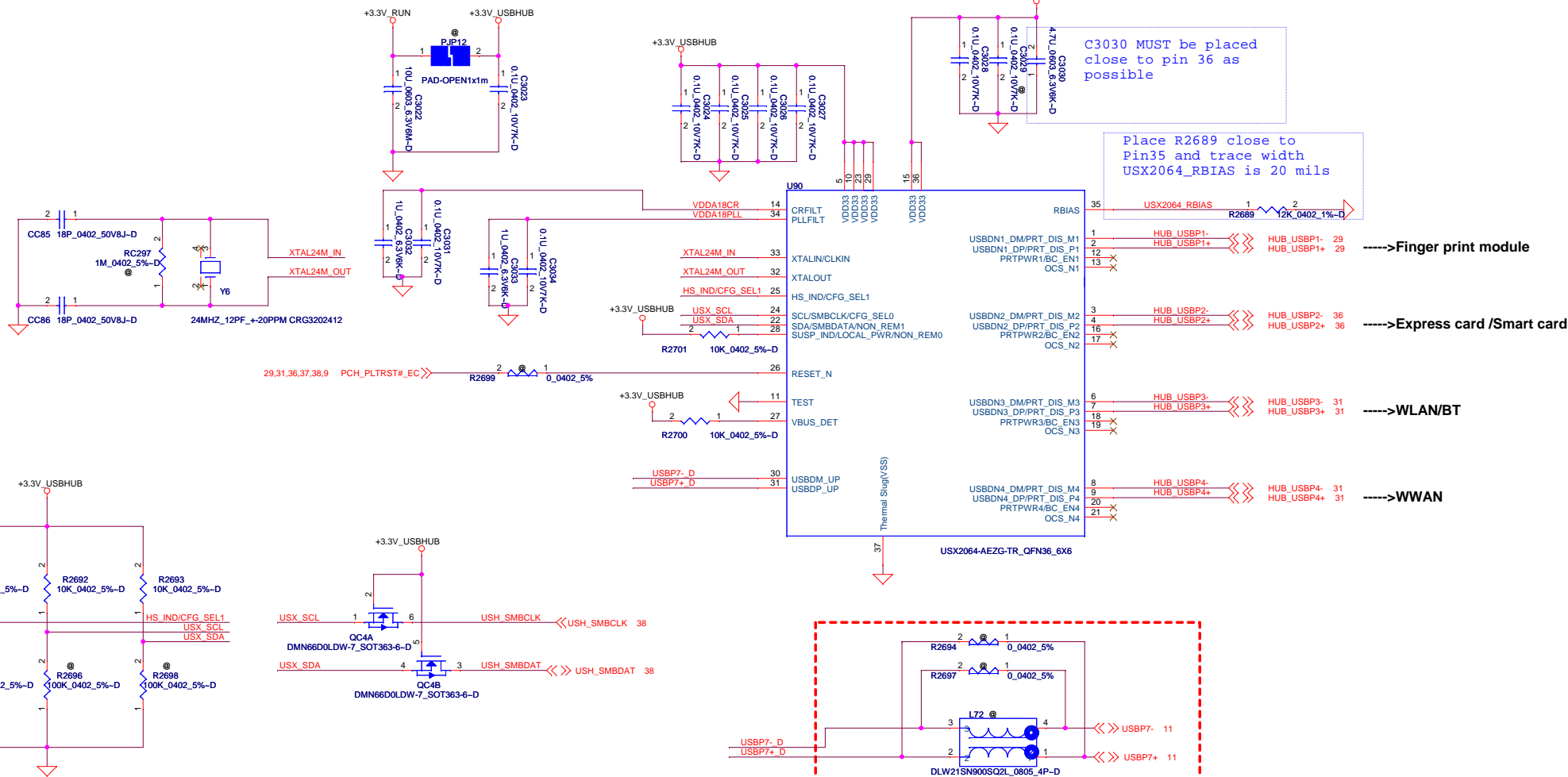
B \ S	EXPRESS_DET#
EXPCLK_REQ#	0
FMCLK_REQ#	1



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		Compal Electronics, Inc.	
		RTC Batt/PCIE SATA SW	
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USX2064 CFG Selection Table

CFG_SEL[0]	0	1
CFG_SEL[1]	Default	SMBus slave device
0	Default	SMBus slave device
1	Bus-powered operation	I2C EEPROM

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USB2.0 HUB-USX2064

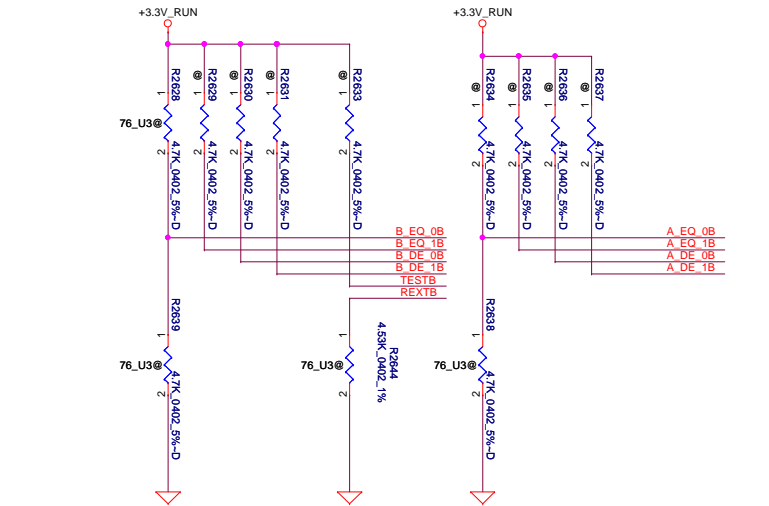
LA-9832P

Rev 0.5

Date: Monday, June 17, 2013

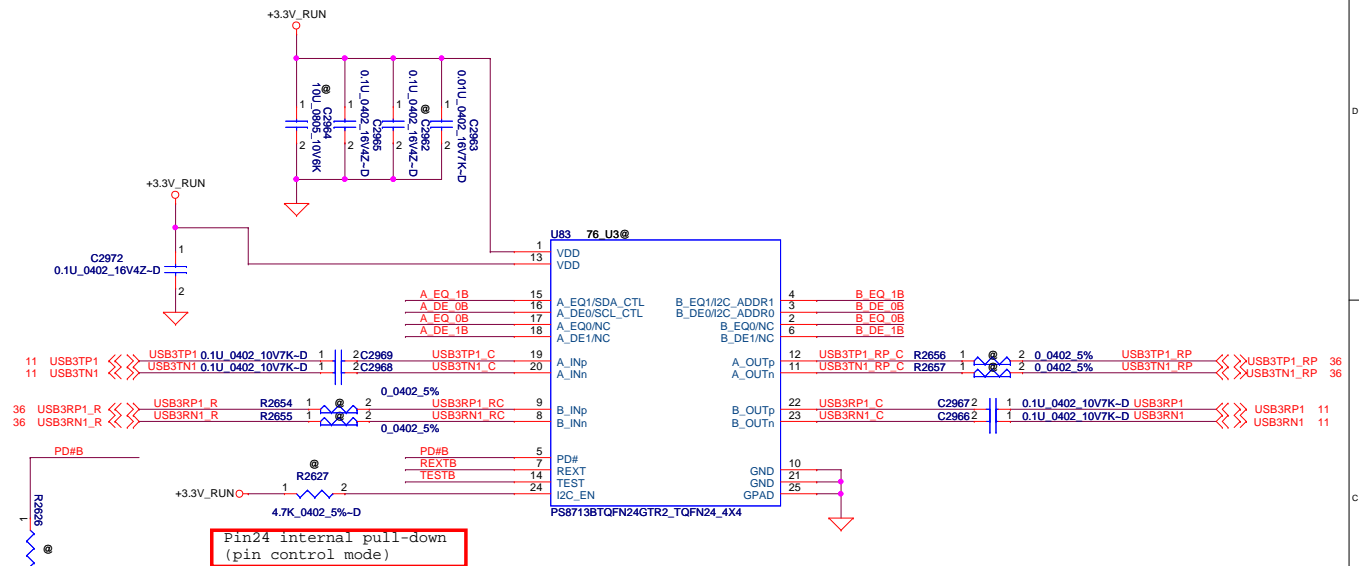
Sheet 33 of 64

USB 3.0 Re-driver for IOB

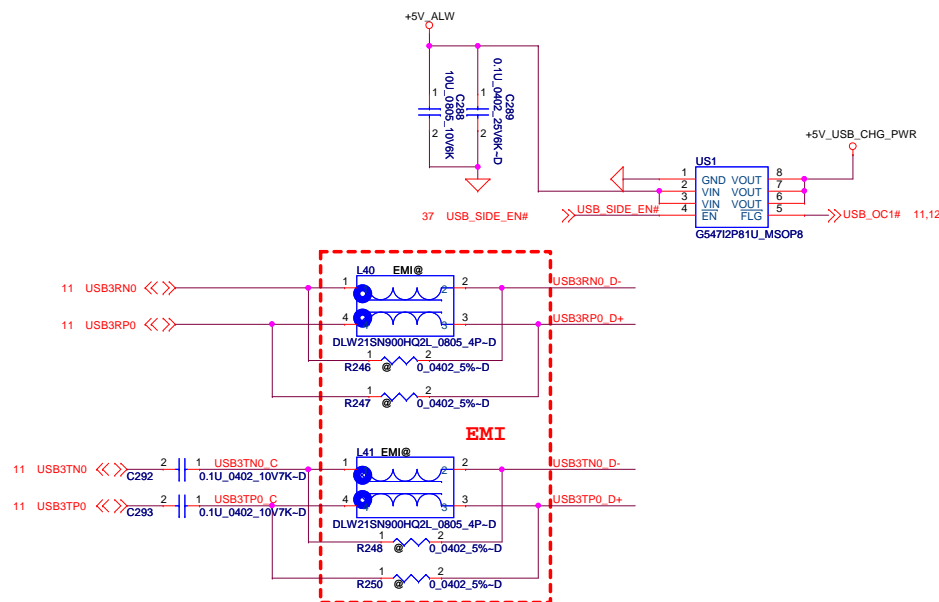
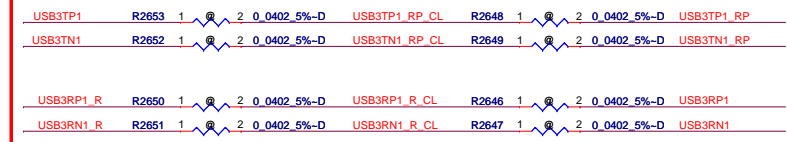


ONLY FOR VAW30

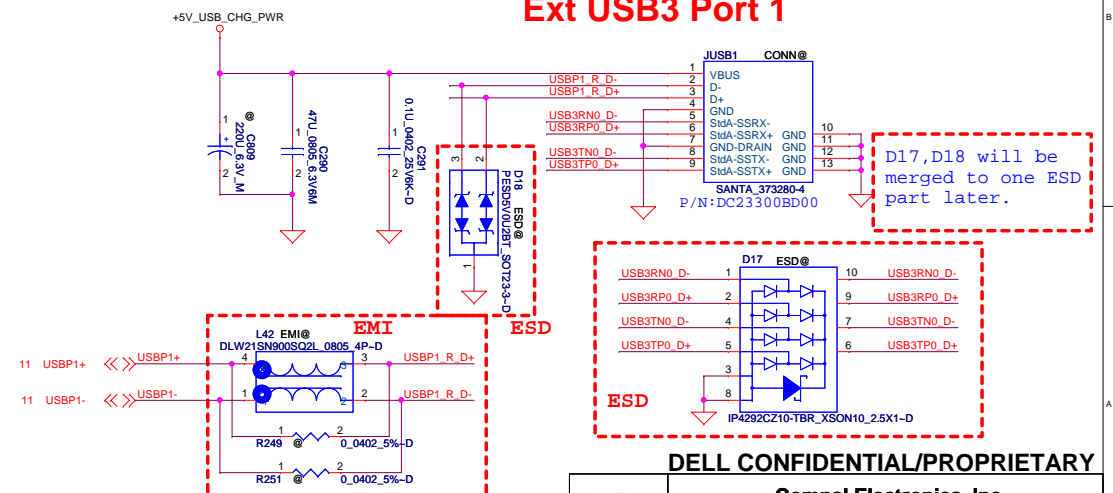
Pericom (Main) SA000006WV00	Parade (2nd) SA000050R20
POP:R2638, R2639	POP:R2628
POP:R2644 (SD000000U200)	POP:R2644 (SD034453180)
A channel EQ 3db DE -3.5db B channel EQ 3db DE -3.5db	A channel EQ 9.5db DE 3.5db B channel EQ 13db DE 3.5db



Co-Layout with PS8713B USB3.0 re-driver



Ext USB3 Port 1



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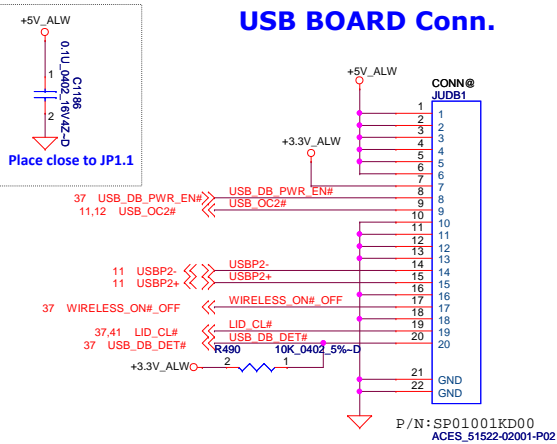
USB on MB/Redriver

Number
LA-9832P

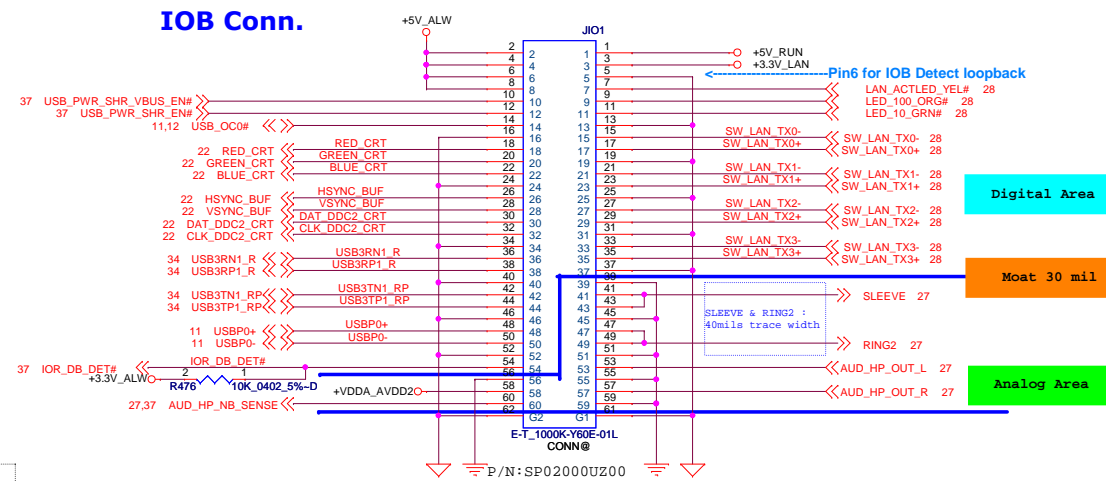
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<div style="text-align: center;">LA-30521</div>		
Date:	Friday, August 30, 2013	Sheet 34 of 64

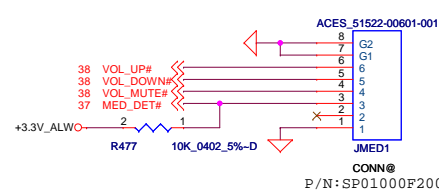
USB BOARD Conn.



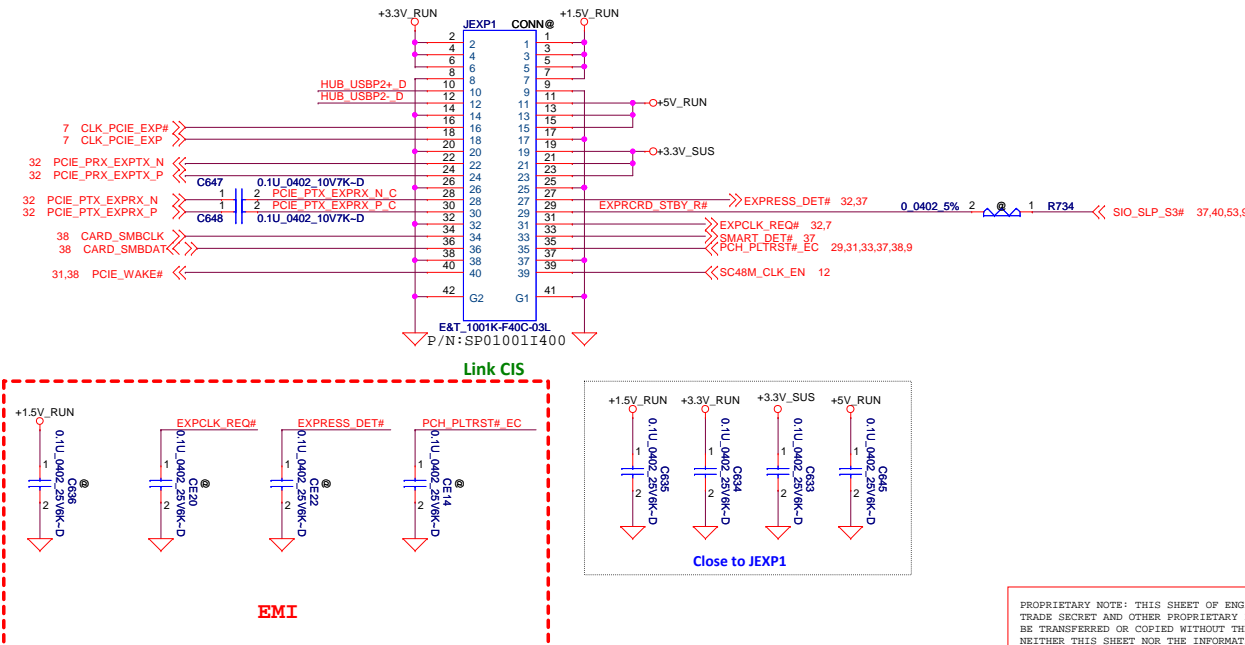
IOB Conn.



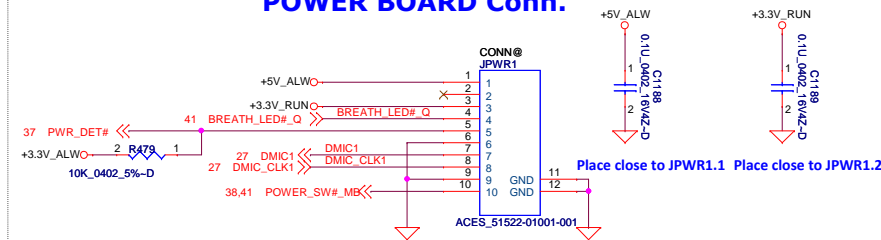
MEDIA BOARD Conn.



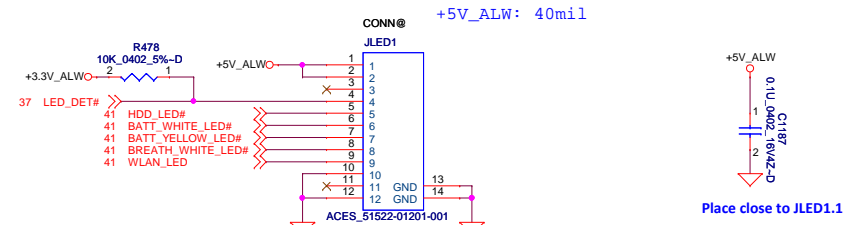
Express/Smart Card Conn.



POWER BOARD Conn.



LED EXTERNAL BOARD Conn.



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I/O Conn

LA-9832P

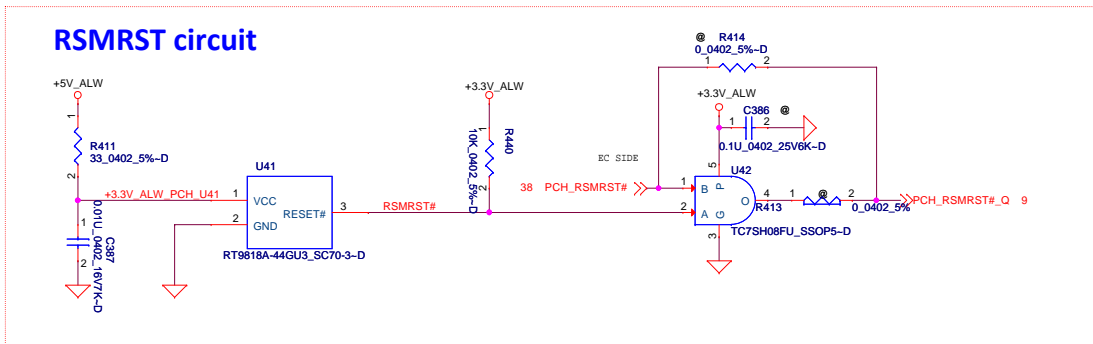
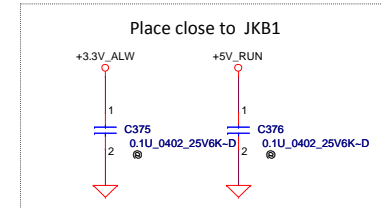
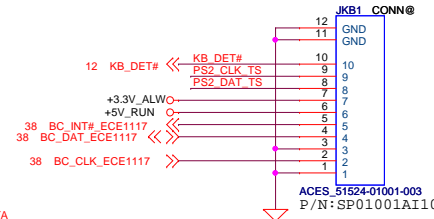
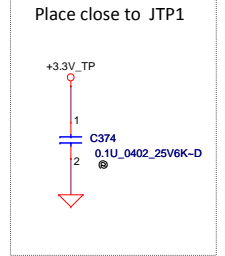
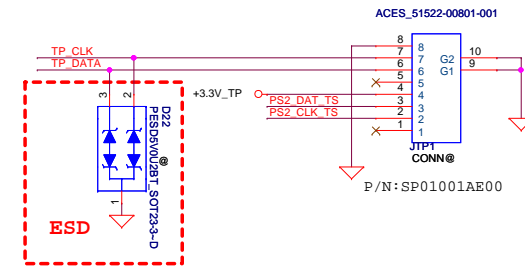
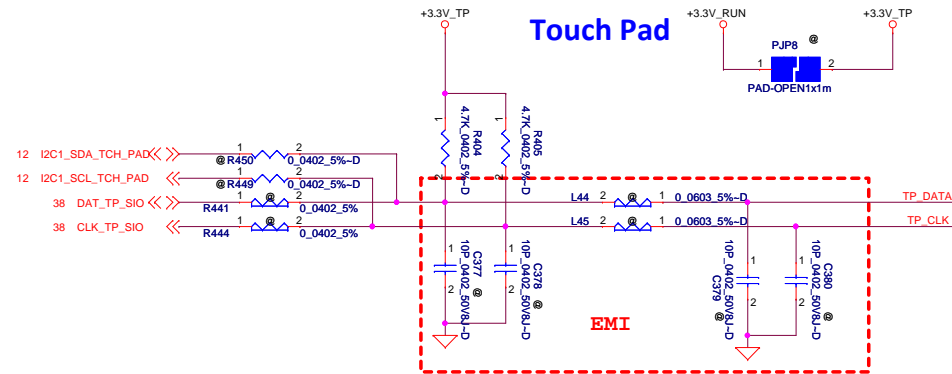
Date: Thursday, August 22, 2013 Sheet 36 of 64

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025	Document Number	LA-9832P	0.5
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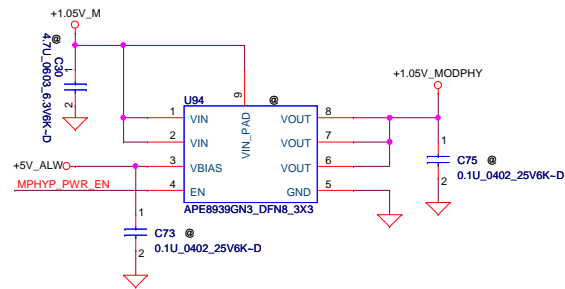
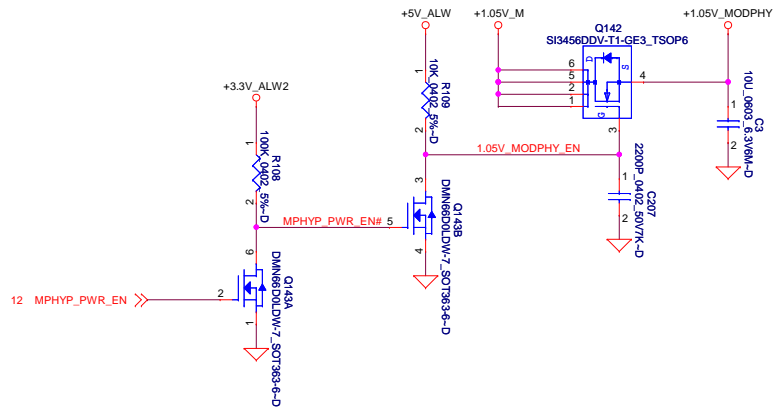


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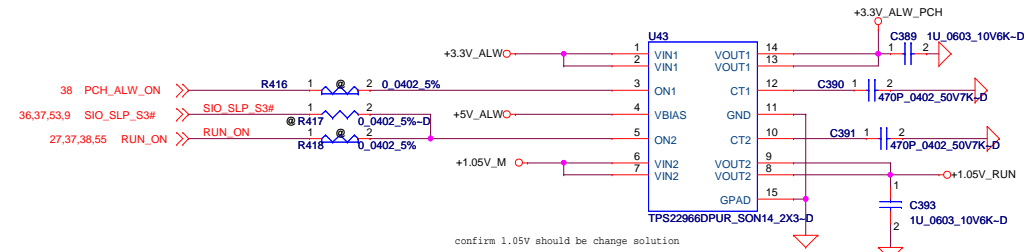
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Size	Document Number	Rev	
	LA-9832P	0.5	
Date	Thursday, June 13, 2013	Sheet	39 of 64

+1.05V_MODPHY source

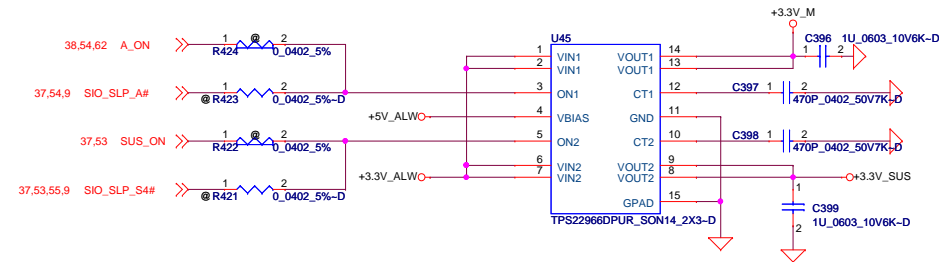


DC/DC Interface

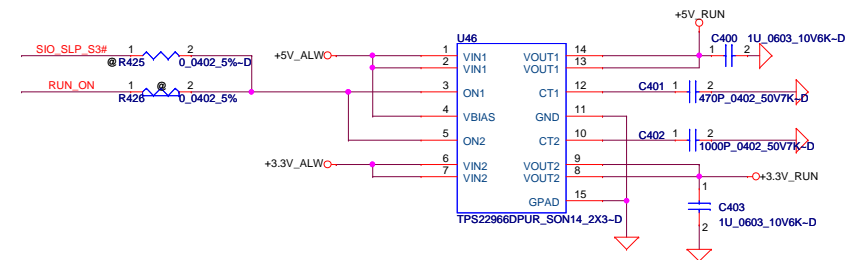
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



DELL CONFIDENTIAL/PROPRIETARY

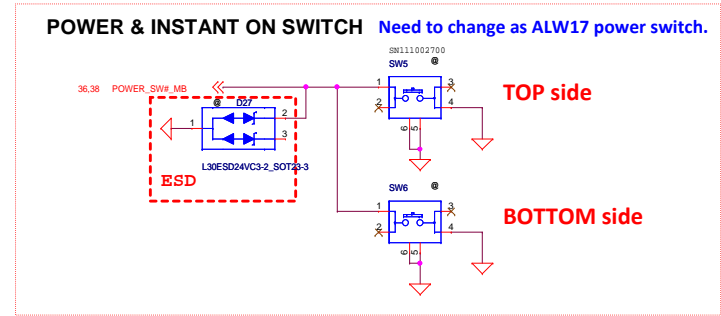
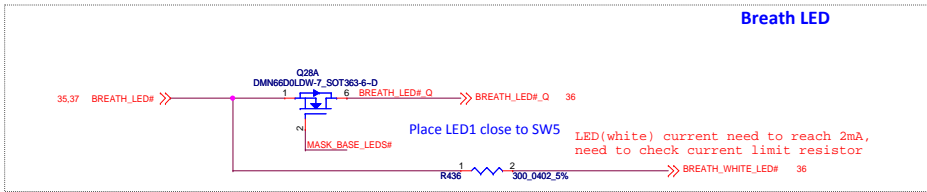
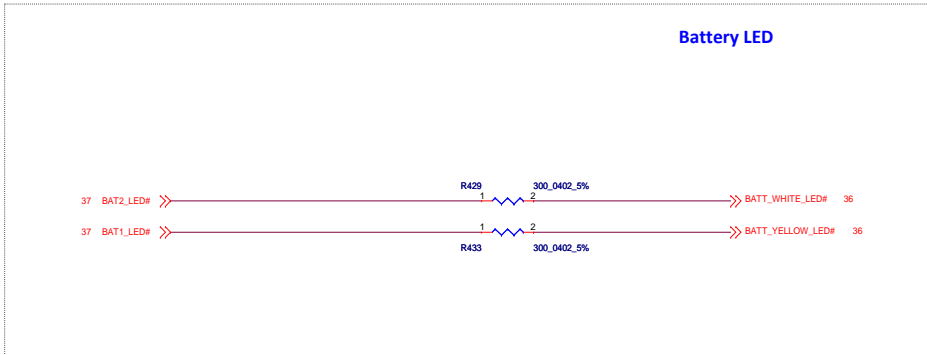
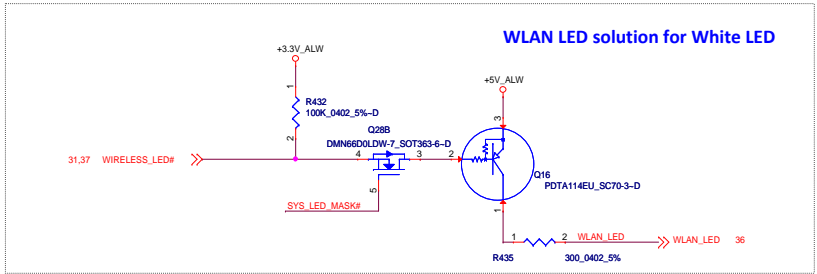
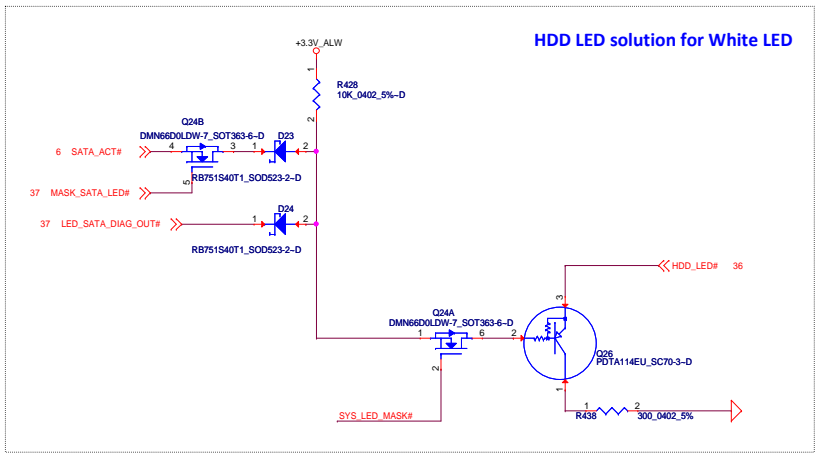
Compal Electronics, Inc.

POWER CONTROL

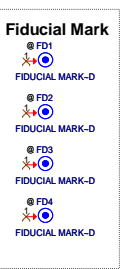
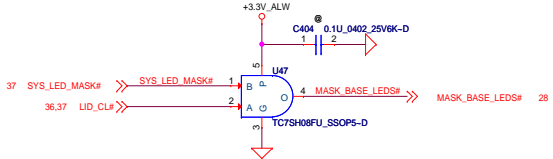
LA-9832P

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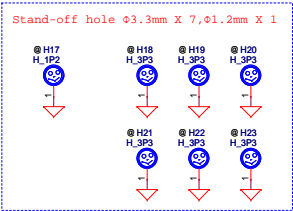
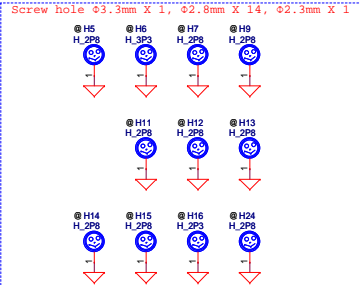
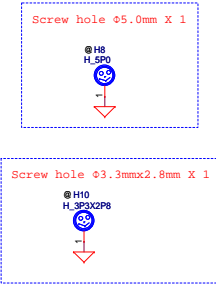
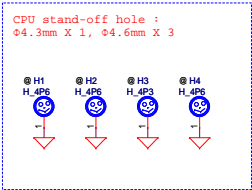
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Lid has been moved to DB.



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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Title: PAD & ME & LED

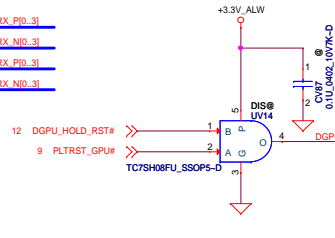
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Date: Wednesday, August 14, 2013

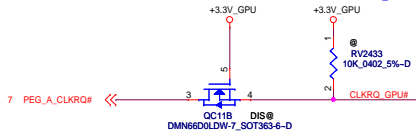
Sheet 41 of 64

Rev 0.5

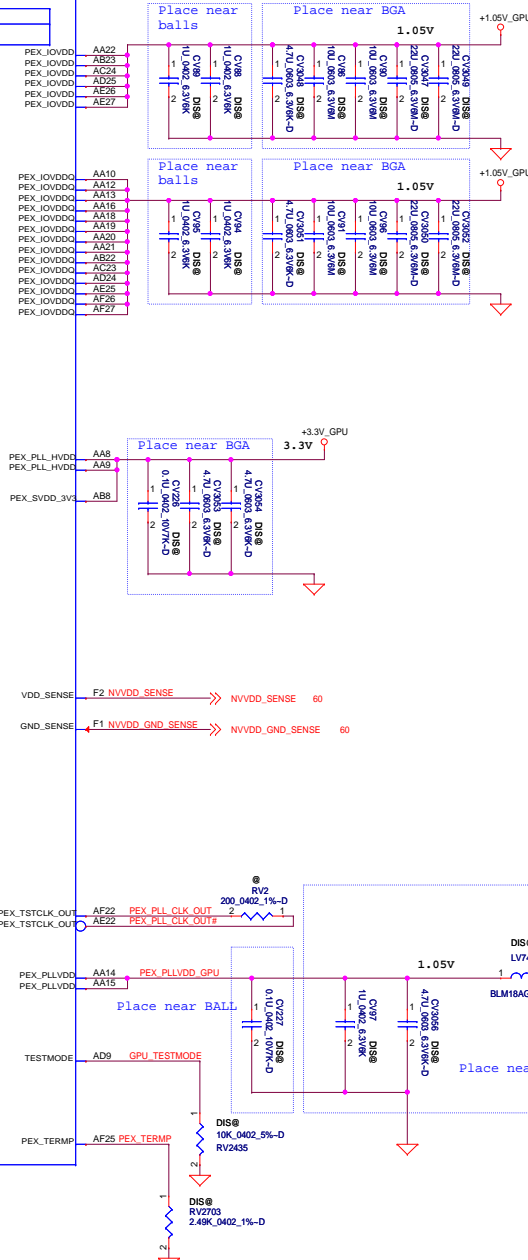
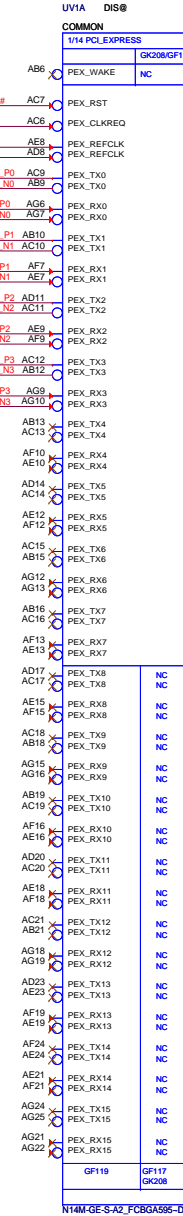
11 PEG_HTX_C_GRX_P[0..3] >> PEG_HTX_C_GRX_P[0..3]
11 PEG_HTX_C_GRX_N[0..3] >> PEG_HTX_C_GRX_N[0..3]
11 PEG_GTX_C_HRX_P[0..3] >> PEG_GTX_C_HRX_P[0..3]
11 PEG_GTX_C_HRX_N[0..3] >> PEG_GTX_C_HRX_N[0..3]



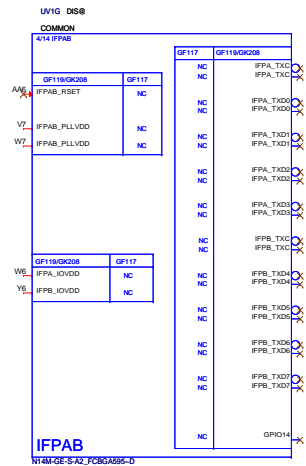
CLK_REQ



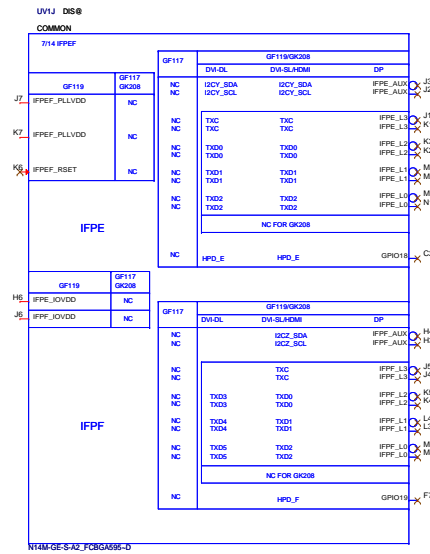
PEG_HTX_C_HRX_P0 0.1U_0402_10V7K-D DIS# 1 2 CV2402 PEG_GTX_HRX_P0
PEG_HTX_C_HRX_N0 0.1U_0402_10V7K-D DIS# 1 2 CV2403 PEG_GTX_HRX_N0
PEG_HTX_C_GRX_P0 0.1U_0402_10V7K-D DIS# 1 2 CV2404 PEG_GTX_HRX_P1
PEG_HTX_C_GRX_N1 0.1U_0402_10V7K-D DIS# 1 2 CV2405 PEG_GTX_HRX_N1
PEG_HTX_C_GRX_P1 0.1U_0402_10V7K-D DIS# 1 2 CV2406 PEG_GTX_HRX_P2
PEG_HTX_C_GRX_N2 0.1U_0402_10V7K-D DIS# 1 2 CV2407 PEG_GTX_HRX_N2
PEG_HTX_C_GRX_P2 0.1U_0402_10V7K-D DIS# 1 2 CV2408 PEG_GTX_HRX_P3
PEG_HTX_C_GRX_N3 0.1U_0402_10V7K-D DIS# 1 2 CV2409 PEG_GTX_HRX_N3
PEG_HTX_C_GRX_P3 0.1U_0402_10V7K-D DIS# 1 2 CV2410 PEG_GTX_HRX_N4
PEG_HTX_C_GRX_N4 0.1U_0402_10V7K-D DIS# 1 2 CV2411 PEG_GTX_HRX_N5



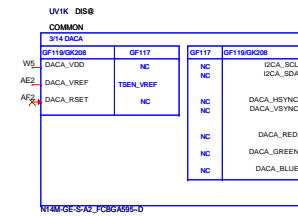
IFPA/B



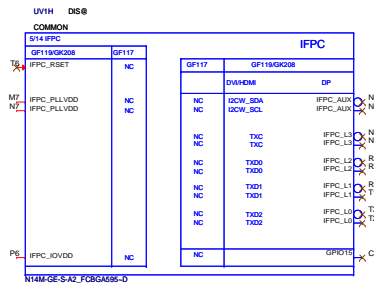
IFPE/F



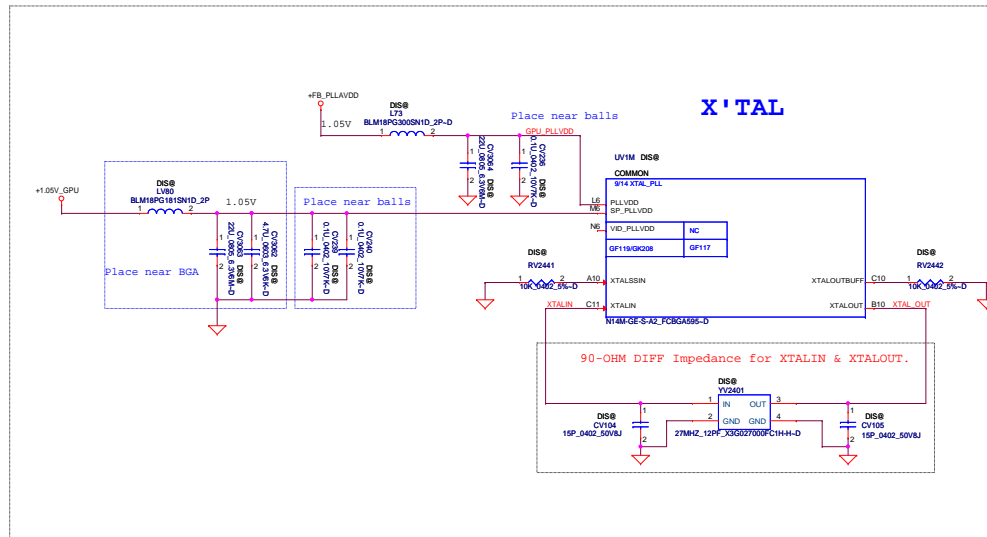
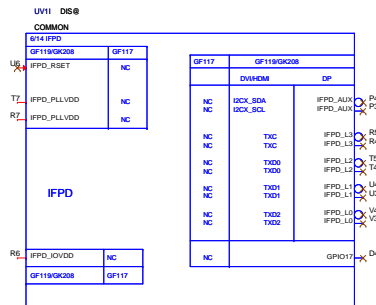
DAC_A



IFPC



IFPD



GPIO

VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded guard tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

For Boundary
Scan using.

UV1N DIS@

COMMON

8/14 MISC1

E12 THERMDN

F12 THERMDP

JTAG_TCK

JTAG_TMS

JTAG_TDI

JTAG_TDO

JTAG_TRST

RV88

10K_0402_5%

DIS@

GPIO0

GPIO1

GPIO2

GPIO3

GPIO4

GPIO5

GPIO6

GPIO7

GPIO8

GPIO9

GPIO10

GPIO11

GPIO12

GPIO13

GPIO14

GPIO15

GPIO16

GPIO17

GPIO18

GPIO19

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GPIO252

GPIO253

GPIO254

GPIO255

GPIO256

GPIO257

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GPIO269

GPIO270

GPIO271

GPIO272

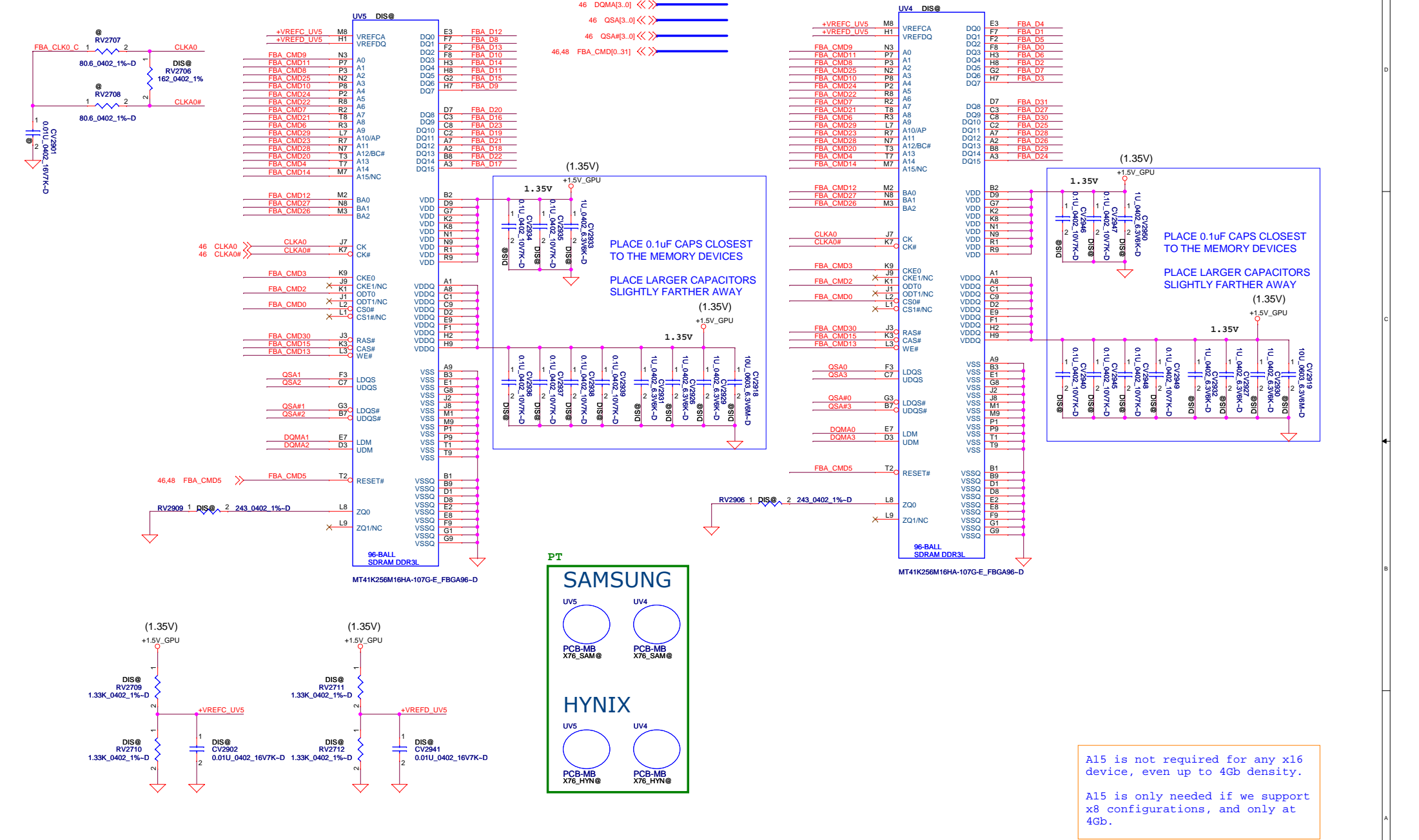
GPIO273

GPIO274

GPIO275

Memory Partition A - Lower 32 bits [31..0]

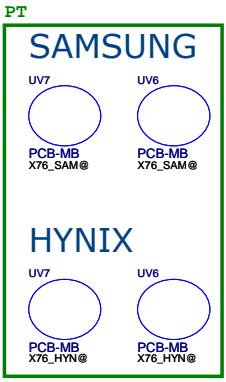
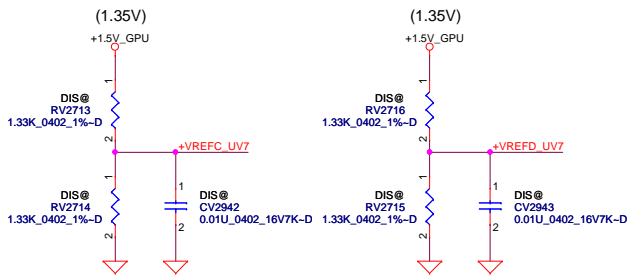
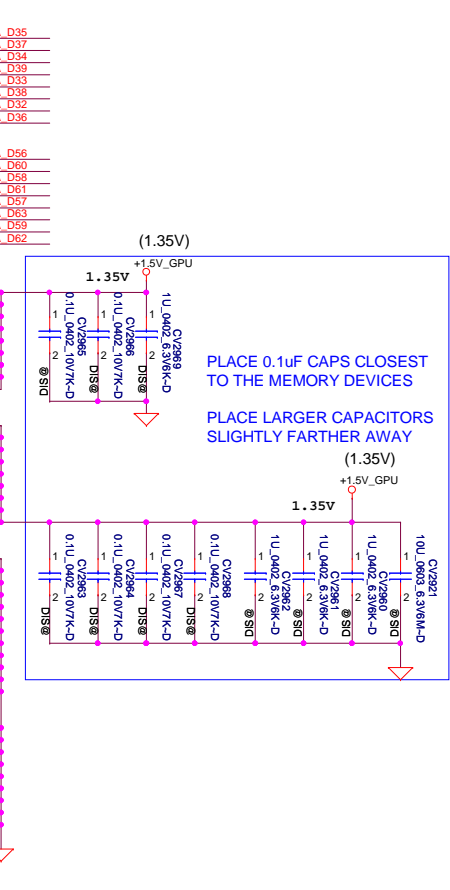
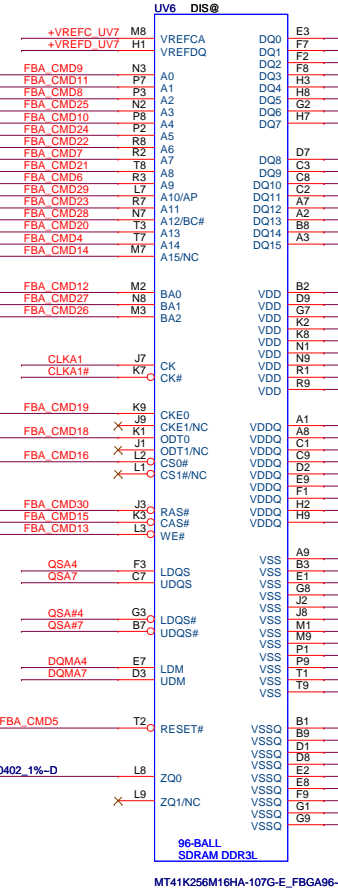
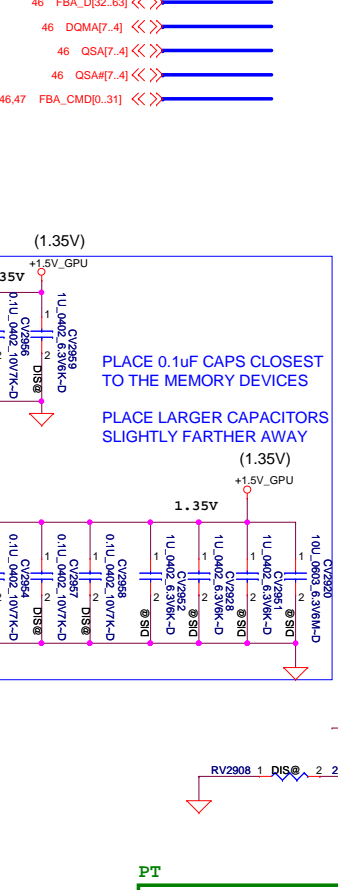
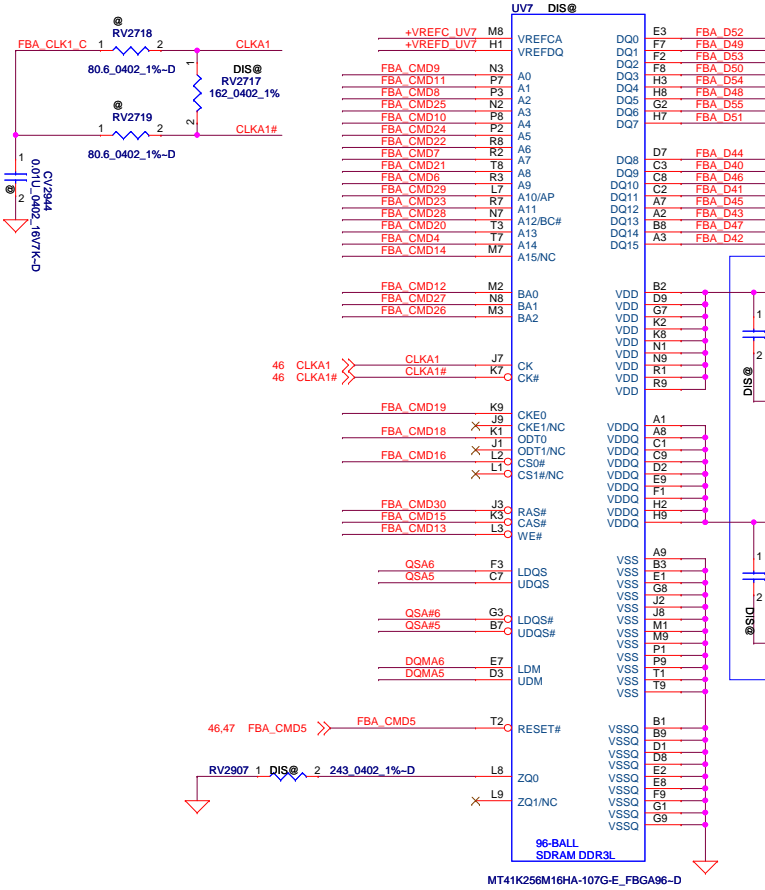
VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E



Memory Partition A - Upper 32 bits [64..32]

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

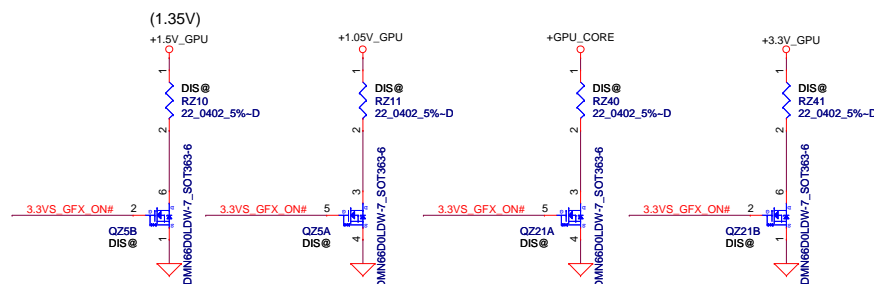
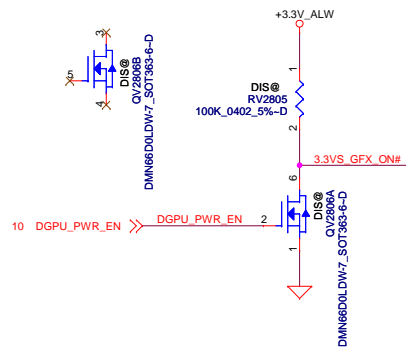
VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E



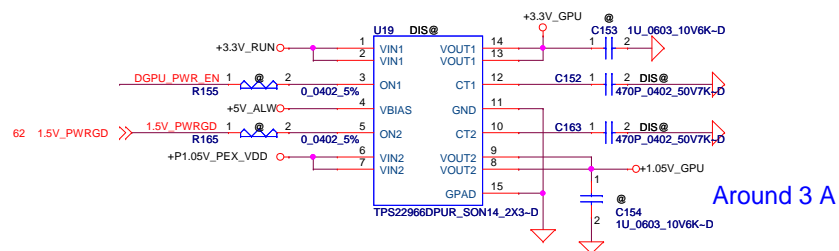
A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

GPU Power Discharge Path

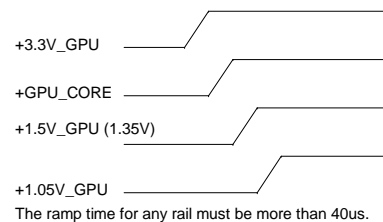


+3.3VRUN to +3.3V_RUN GFX

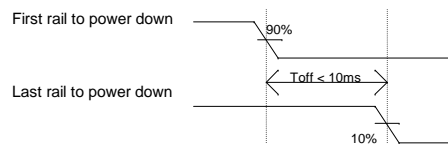


+1.05V_MP to +1.05V_PEX_VDD

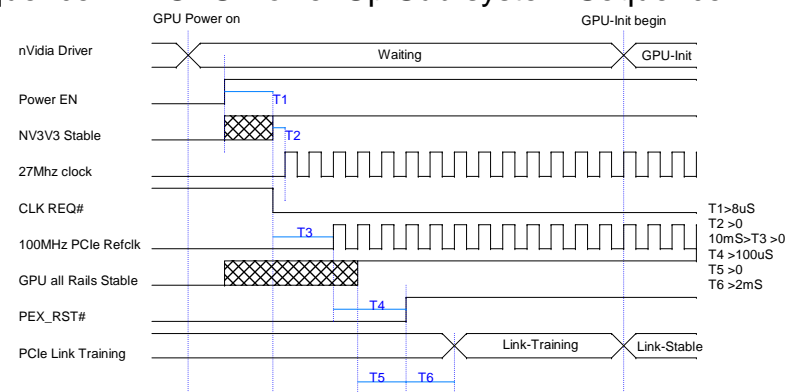
GPU Power Up Power Rail Sequence



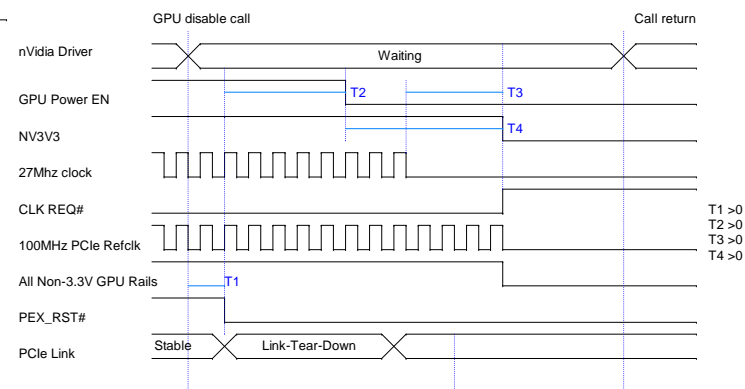
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence




Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA DC/DC Interface	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	
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				Document Number	
Date: Thursday, August 15, 2013				Sheet 49 of 64	

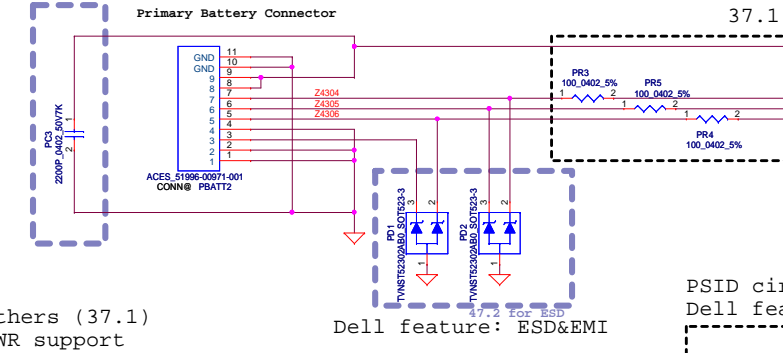
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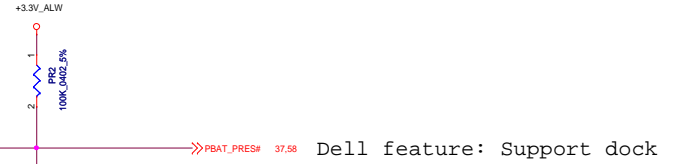
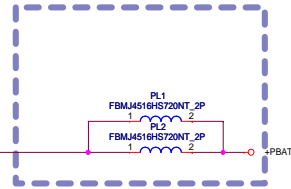
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			Compal Electronics, Inc.		
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	LA-9832P		0.5		
Date:	Thursday, June 13, 2013		Sheet	50	of 64

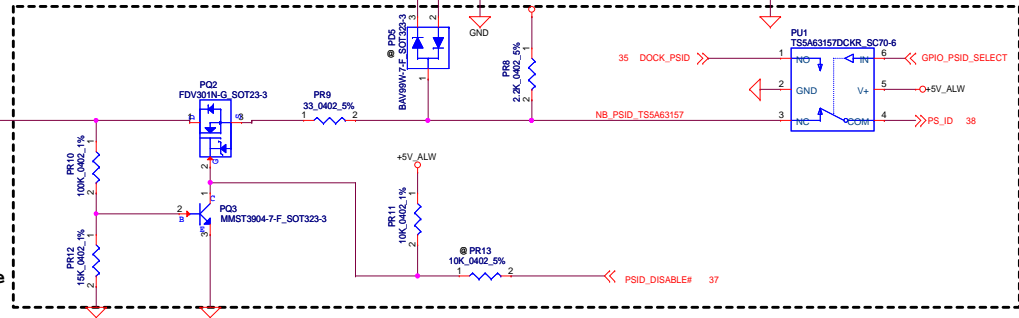
EMI (47.1)



EMI (47.1)
Dell feature: ESD&EMI



PSID circuit (39.1)
Dell feature: PSID

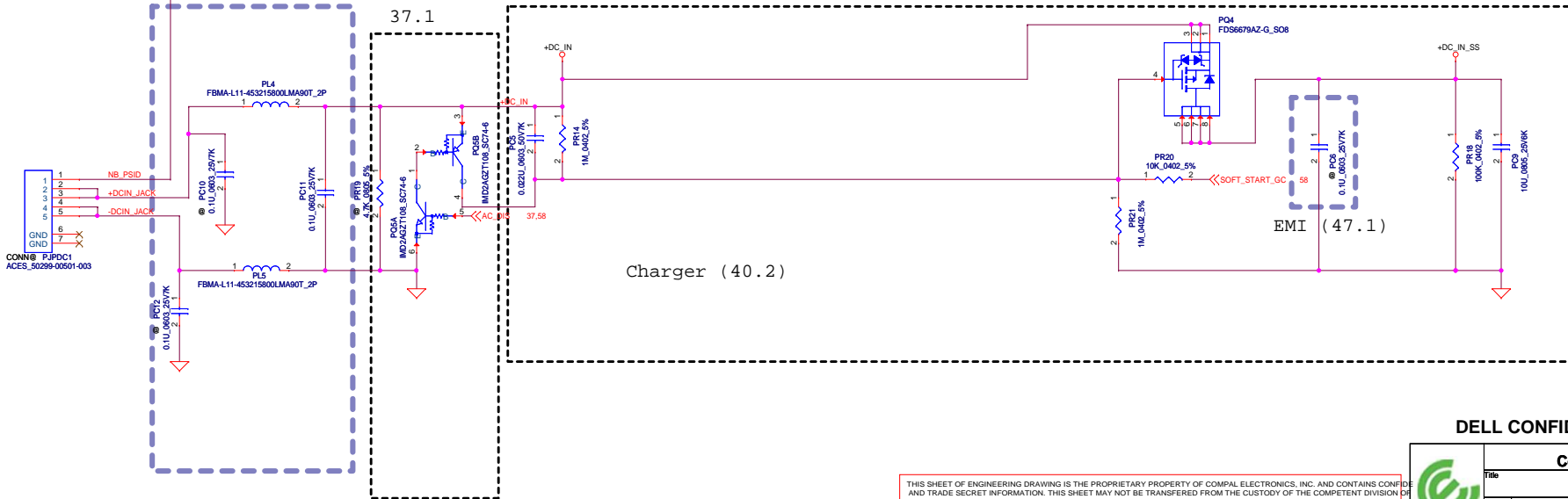


DC_IN+ Source

Dell feature
peak power

37.1

EMI (47.1)



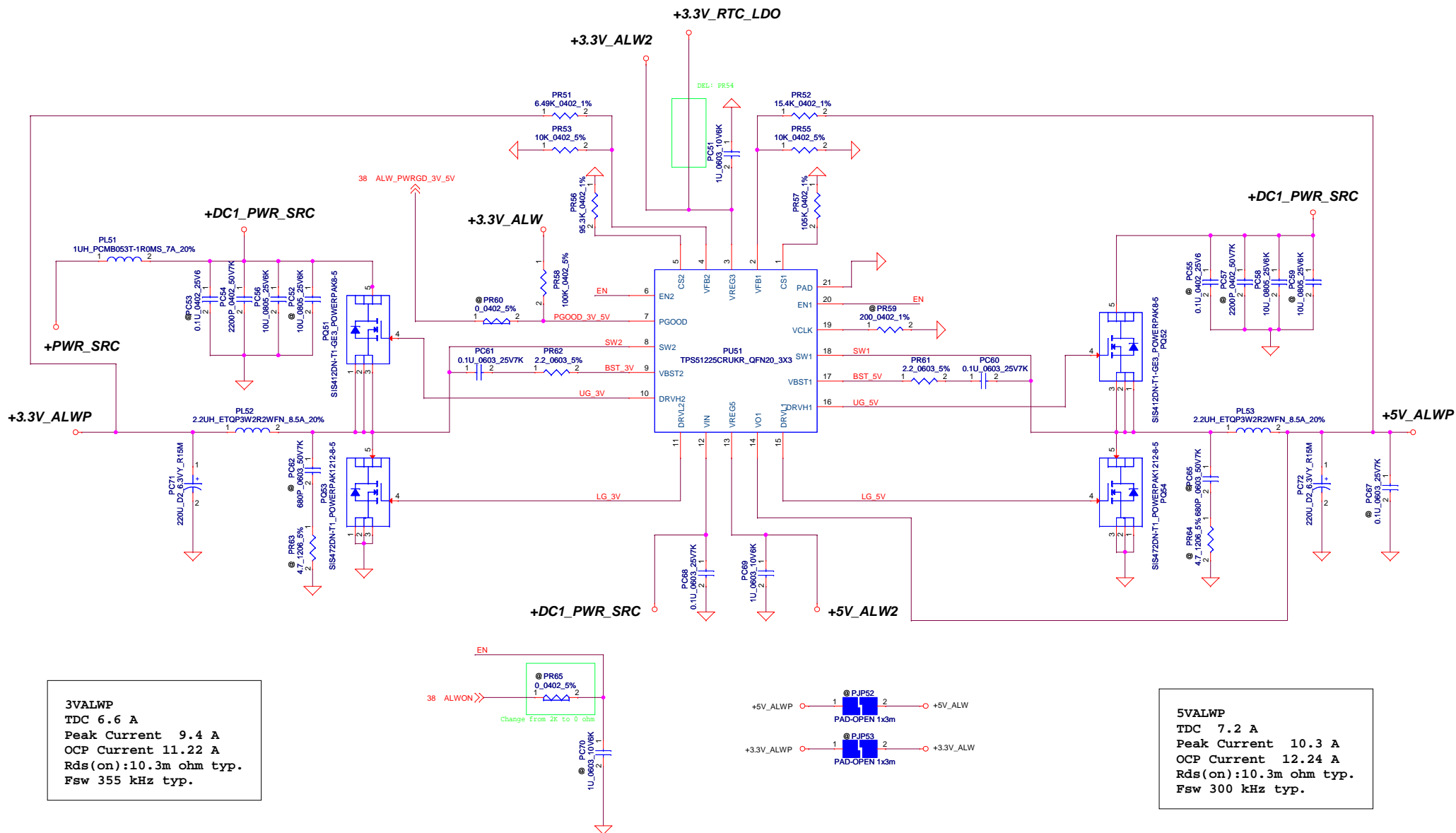
Charger (40.2)

EMI (47.1)

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Title	Document Number	LA-XXXX	Rev 0.1
Date: Wednesday, August 14, 2013	Sheet 51	of 64	

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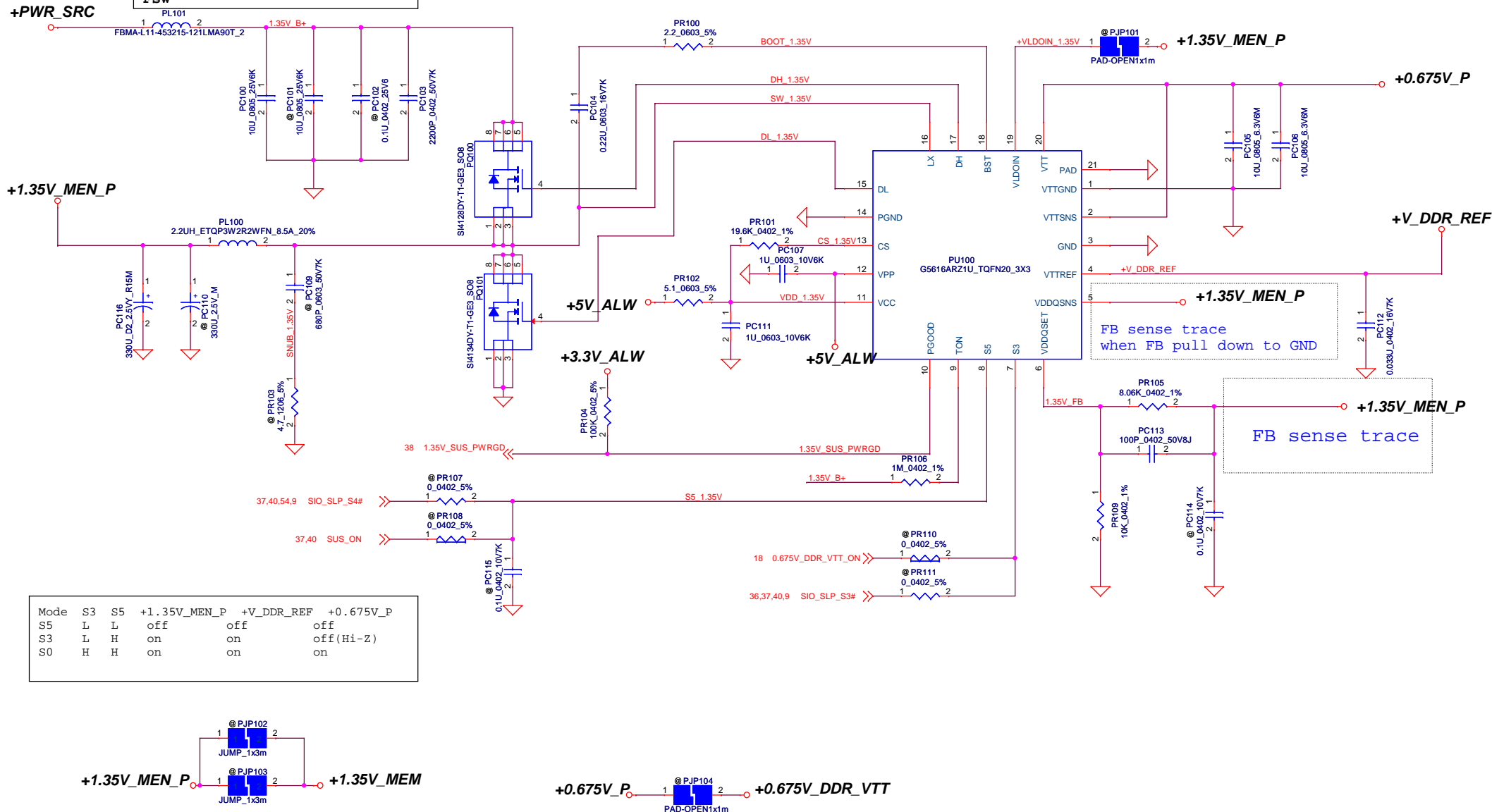
Compal Electronics, Inc.

PWR +5V_ALW/3.3V_ALW

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1.35Volt +/- 5%
TDC: 7.2 A
Peak Current: 10.3 A
OCP current: 12.24 A
Rds(on):14.5m ohm typ
Fsw

0.675Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.8925A

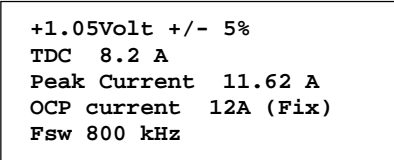



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Title			PWR_+1.35V_MEN/+0.675V_DDR	
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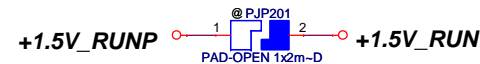
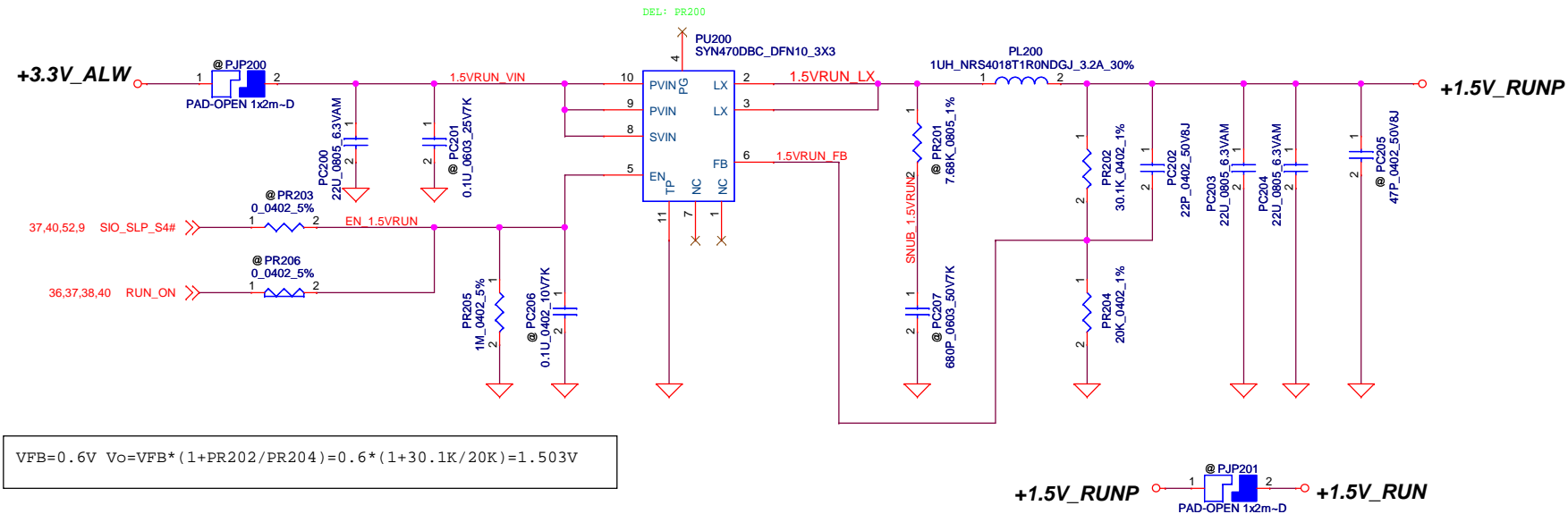
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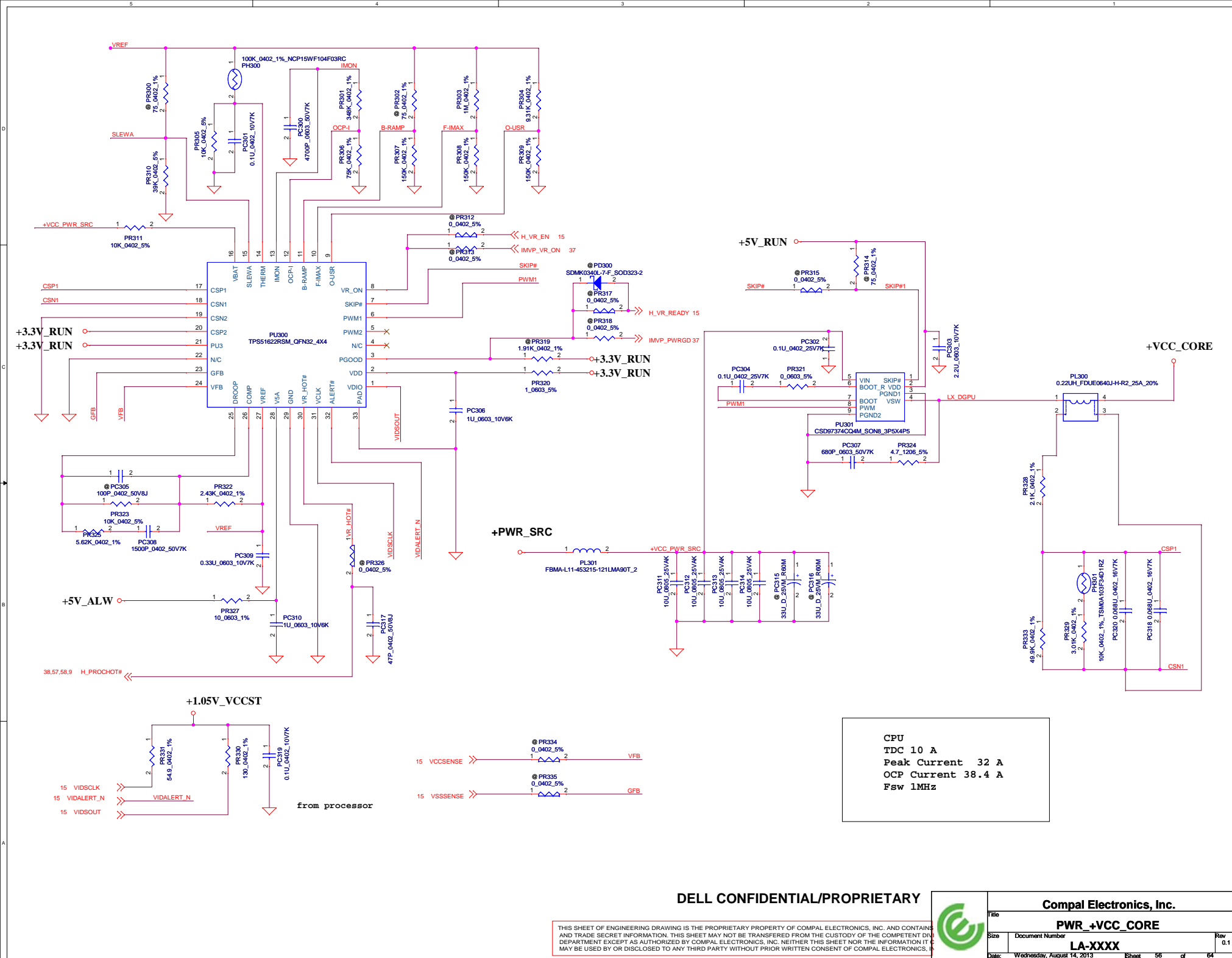
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	Title			
	PWR_+1.05VTPP			
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1.5Volt
Frequency 1MHz
TDC 0.65A
Peak Current 0.93A
OCP current 3.5A (Fix)



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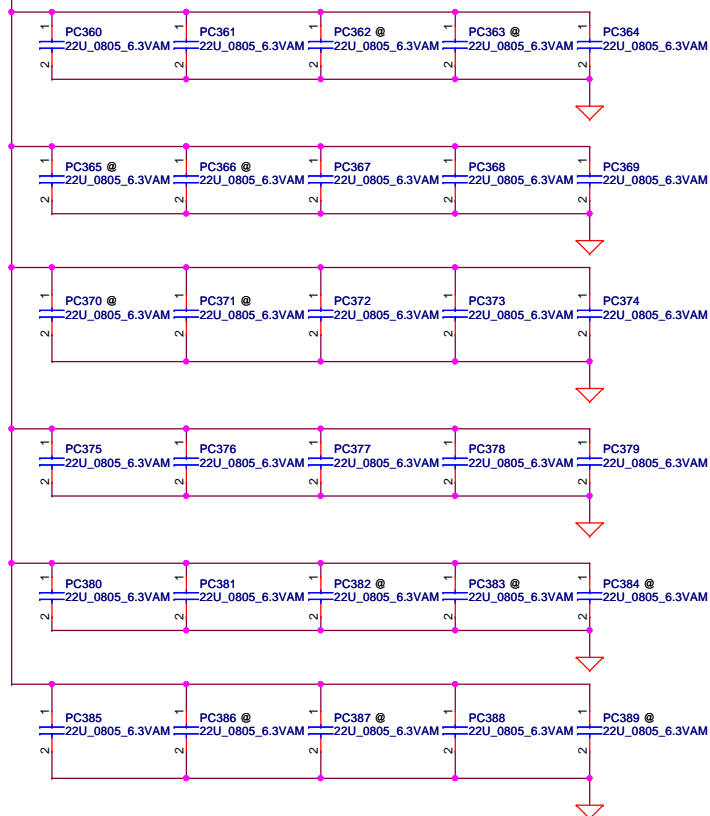
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File	PWR_+VCC_CORE		
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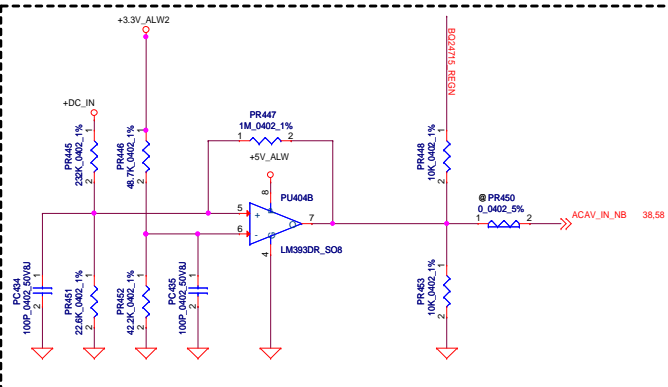
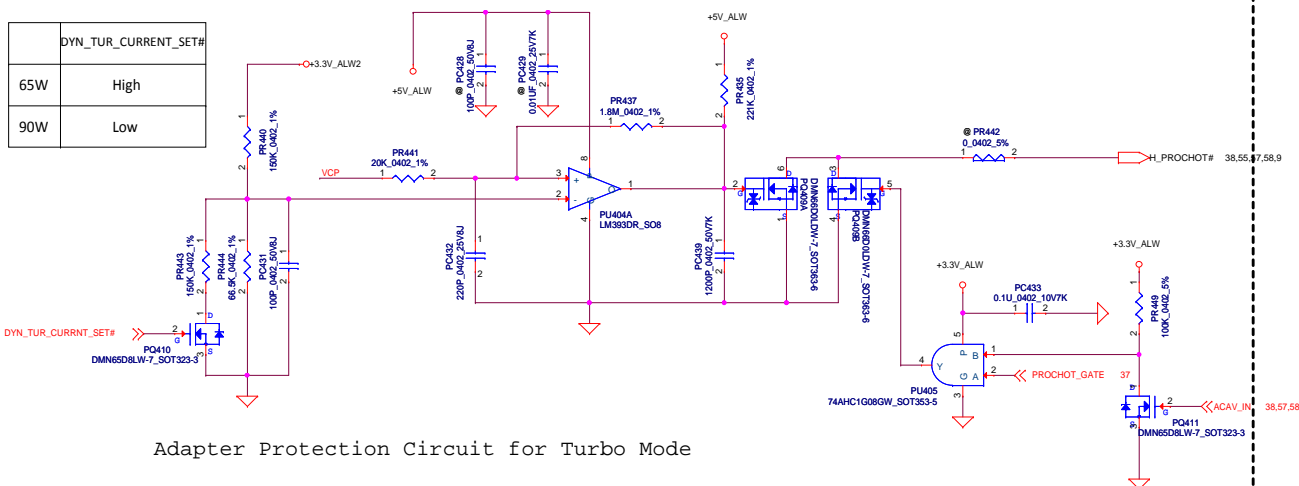
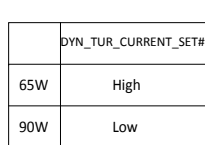
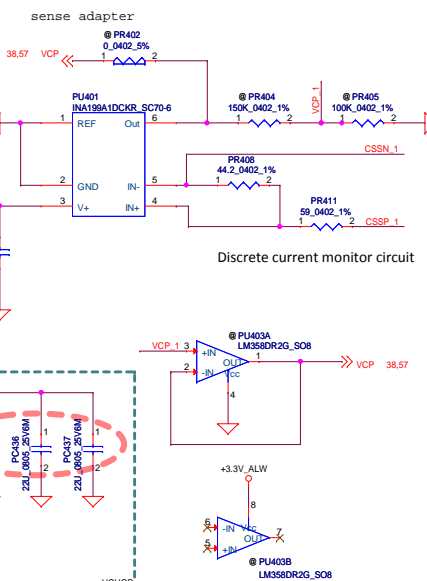
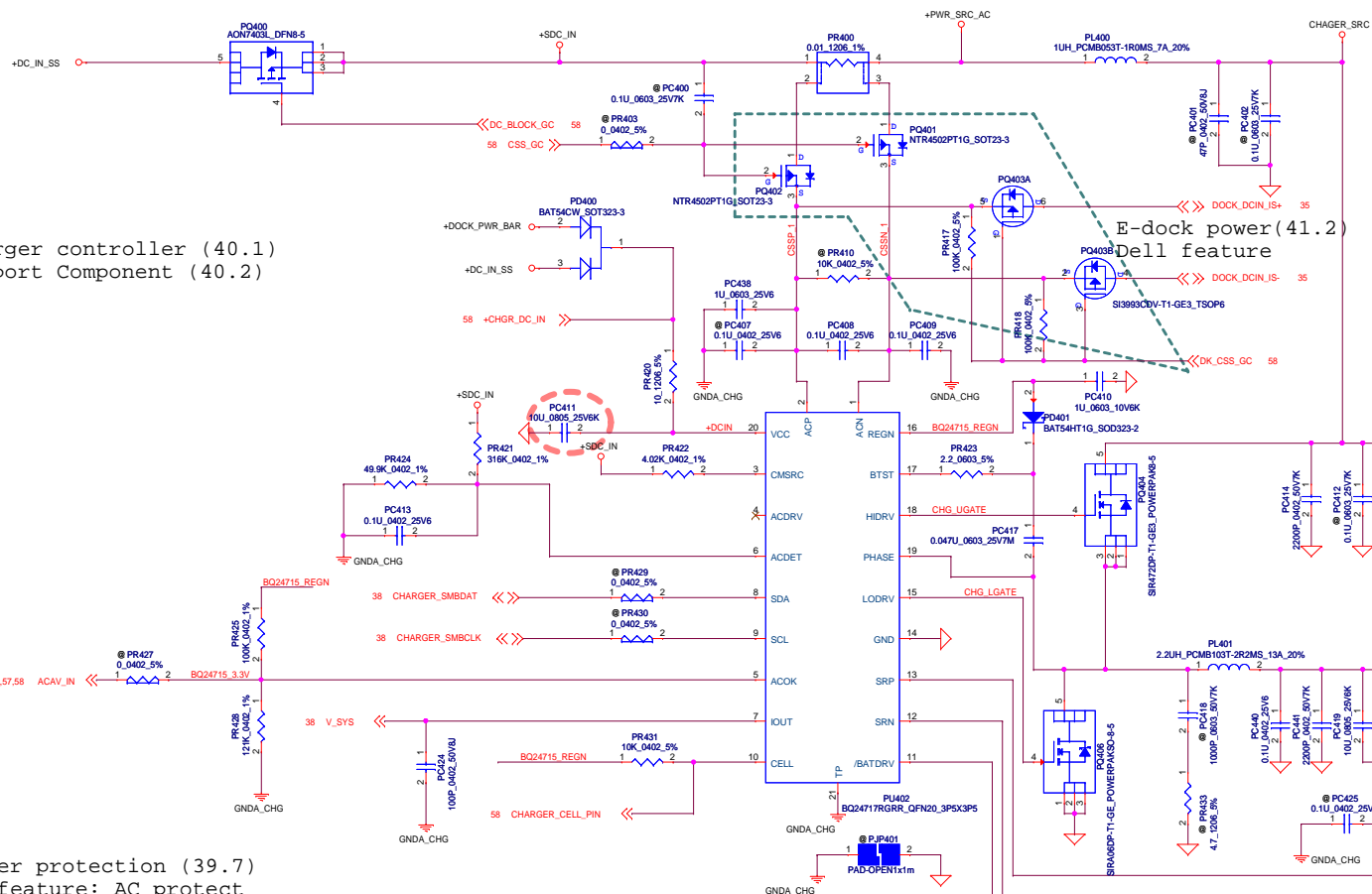
+VCC_CORE



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Title		
PWR_PROCESSOR DECOUPLING		
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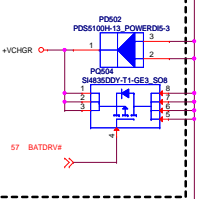
PWR_Chager

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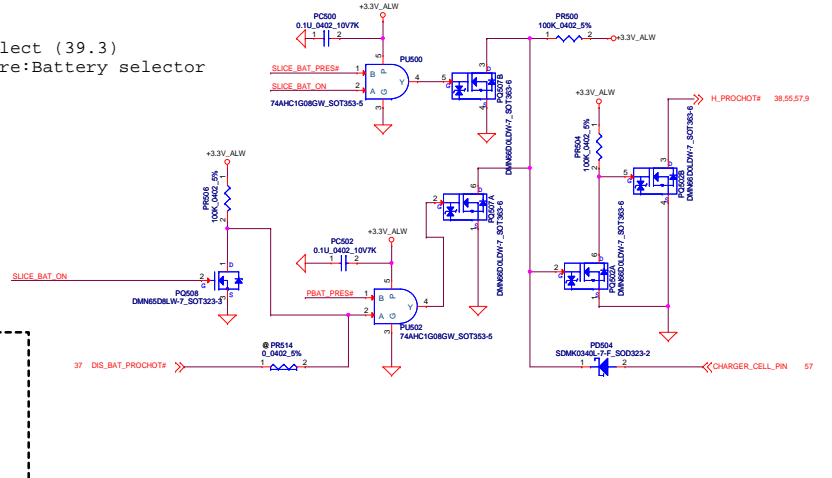
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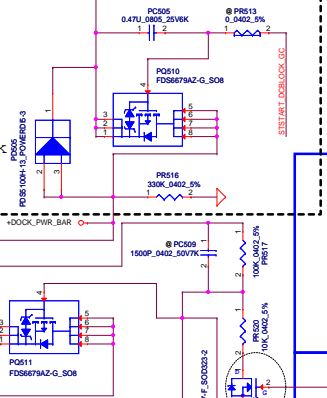
Charger (40.2)



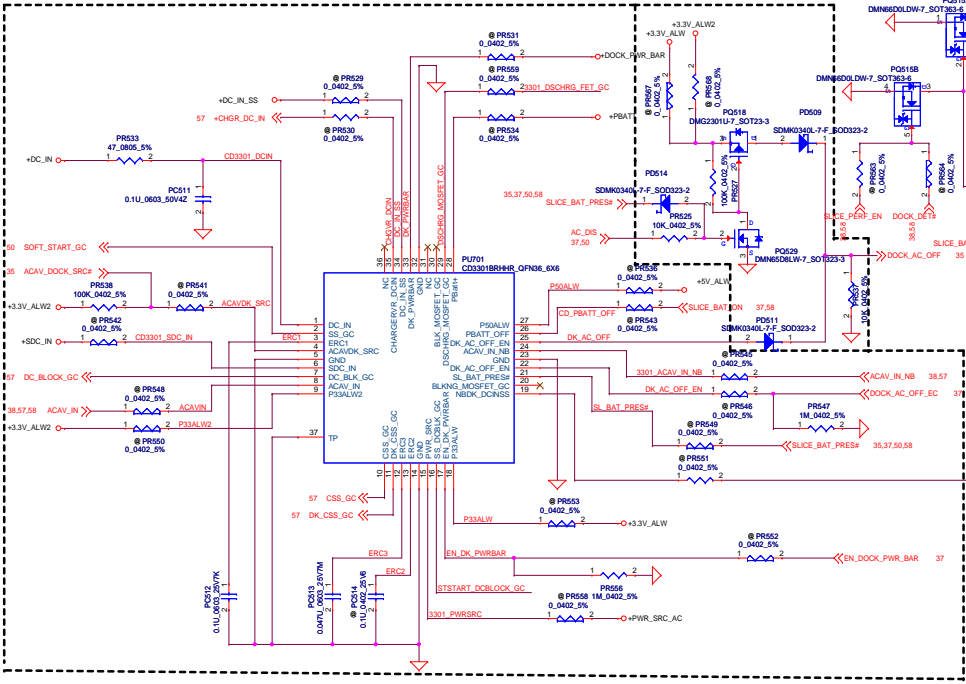
Battery select (39.3)
Dell feature: Battery selector



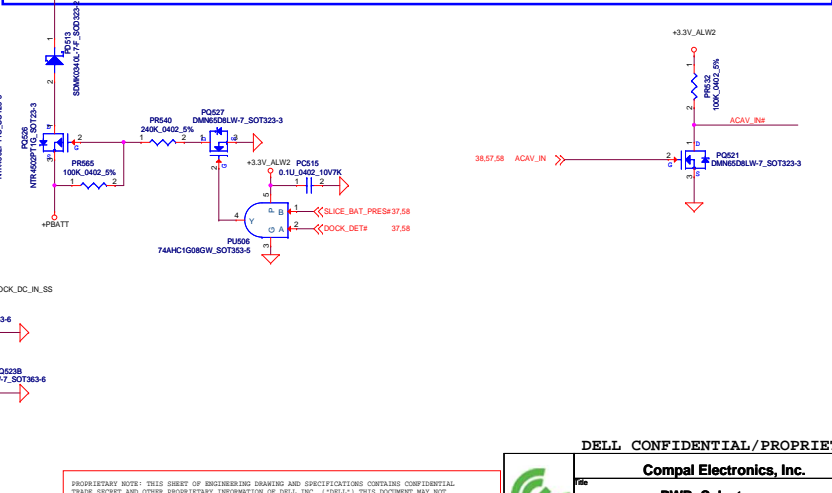
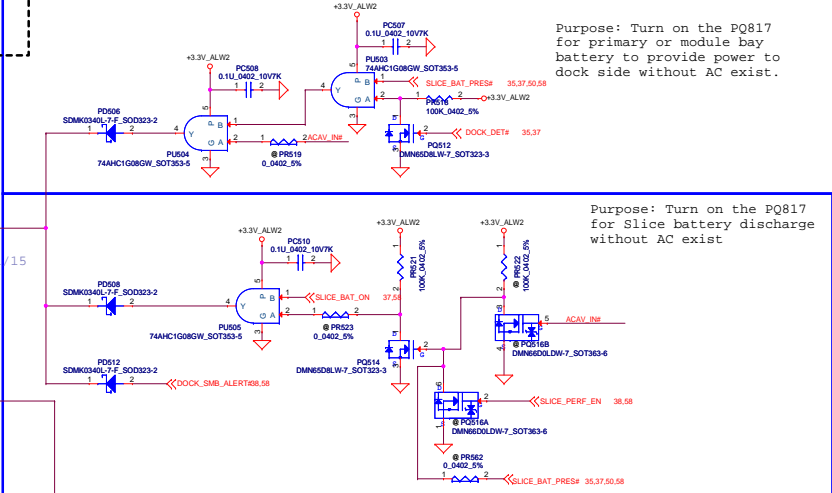
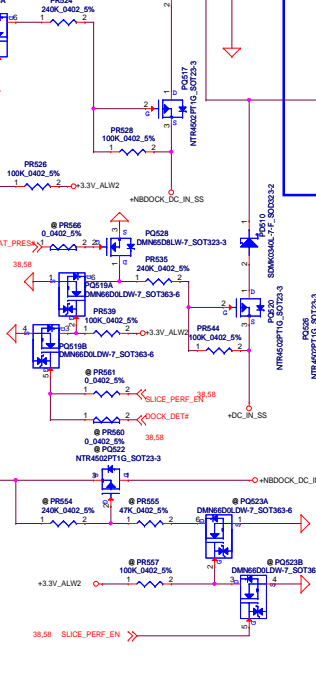
E-dock power(41.2)
Dell feature: Support dock



Edock controller(41.1), support component(41.2)
Dell feature: Support dock



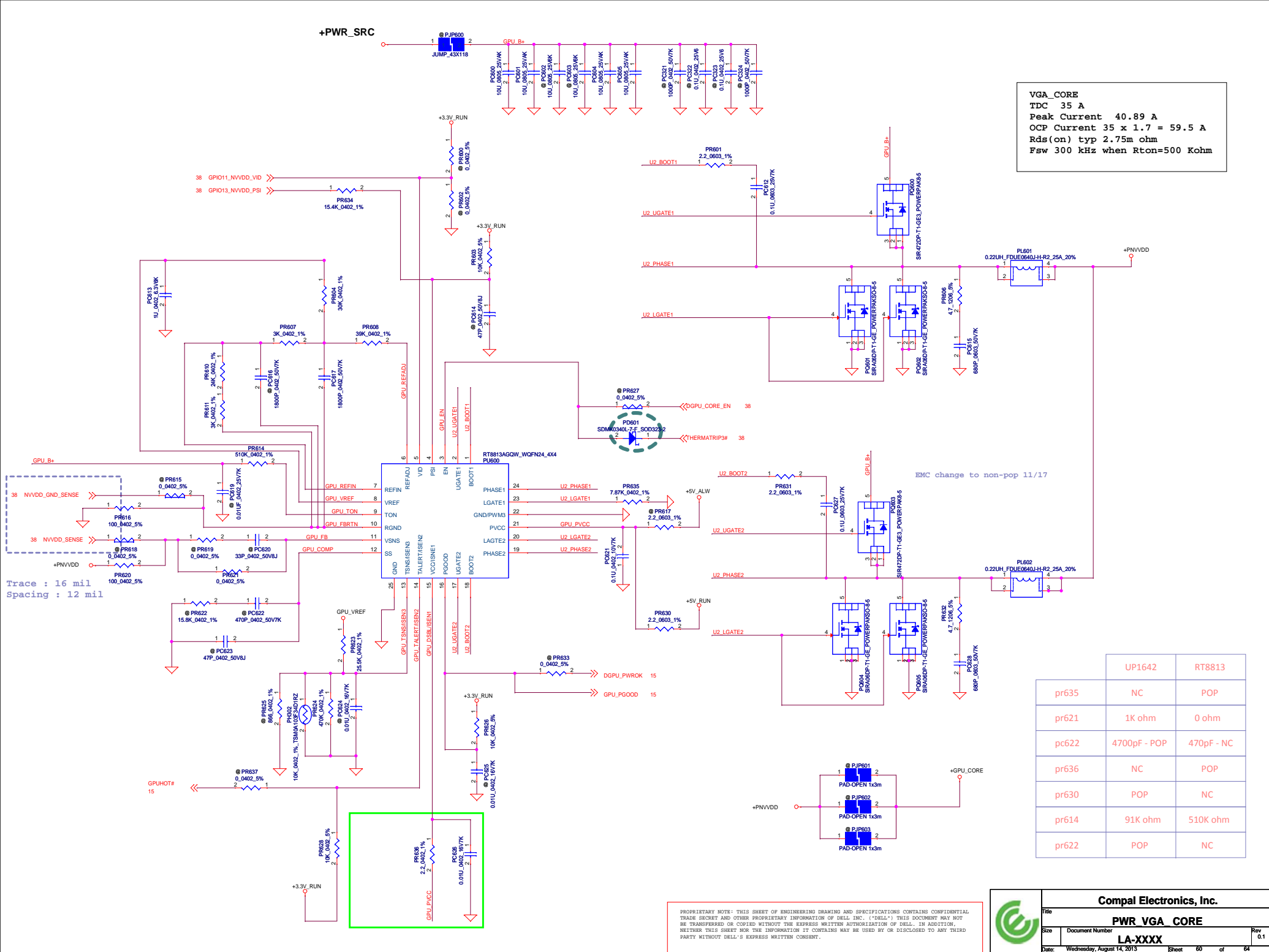
Charger (37.1)
Dell feature: Peak power

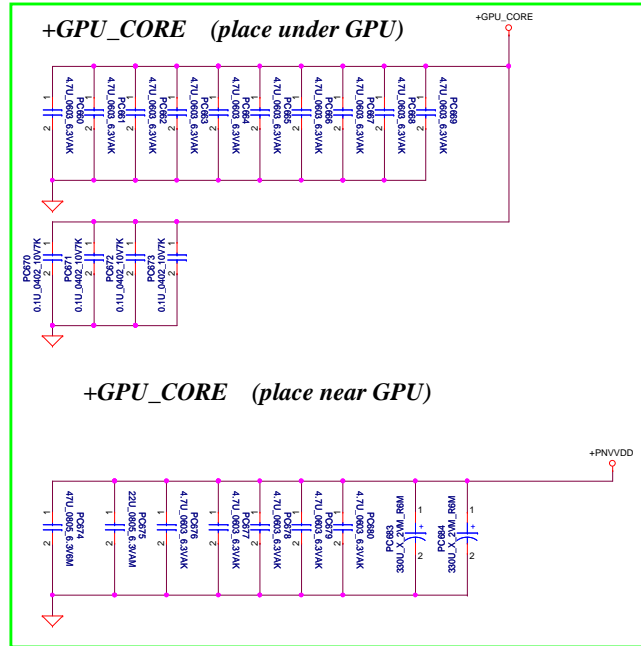


Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.


Purpose: Turn on the PQ817 for Slice battery discharge without AC exist

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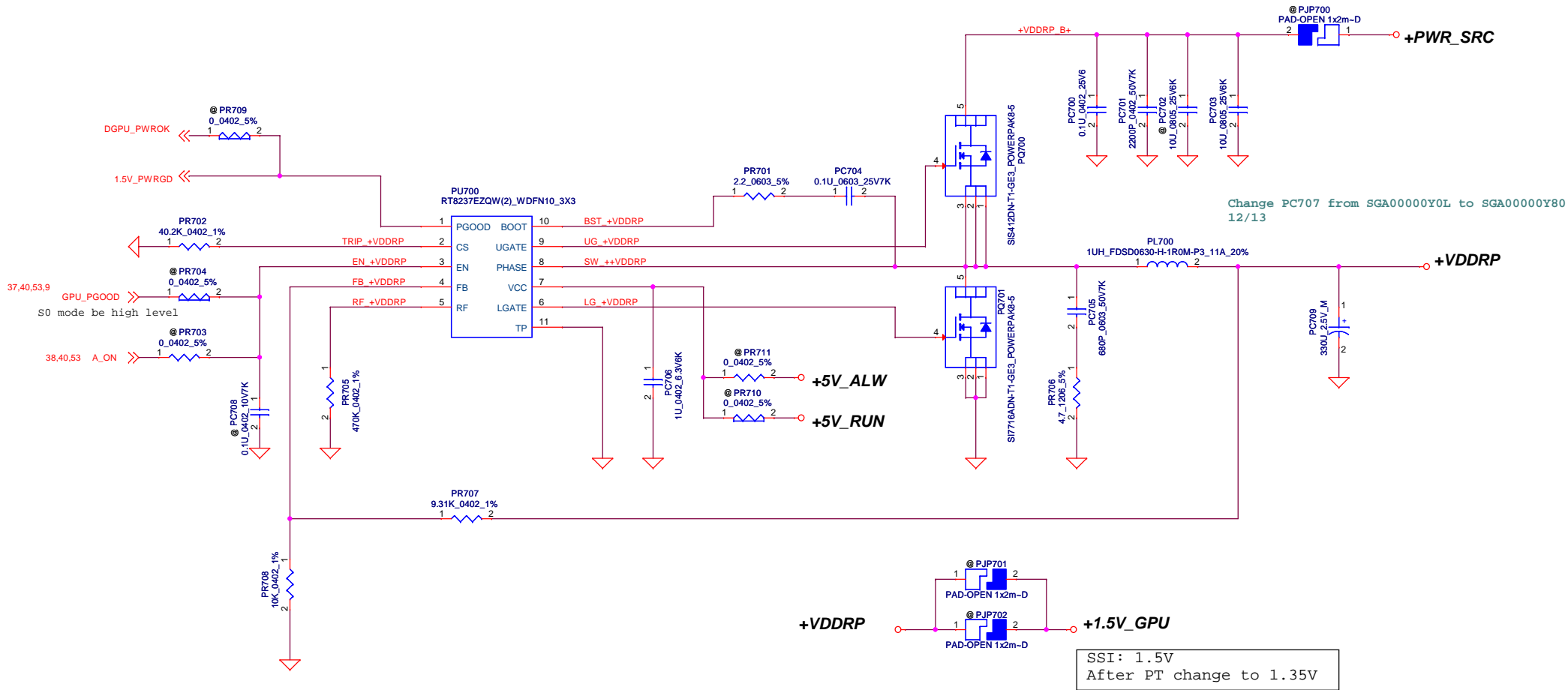
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PWR_GPU_DECOUPLING

LA-8821P

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+VDDRP(1.35V)
TDC 2.94A
Peak Current 4.2A
OCP current 5A
Rds(on):13.5m ohm typ
Fsw 290 kHz when Rrf=470 Kohm

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	58	Adapter Protection Circuit	2013/1/30	Power	PC432 220pF is not popular part	Change to 0402 size	X00
2	59	P59-PWR_Selector	2013/2/4	Power	Battery voltage leakage to docking if only battery	Add: PD513, PQ526, PR565, PR540, PQ527, PU506, PC515	X00
3	56	Vcore fine tune	2013/2/7	Power	Vcore fine tune	Modify: PR306, PR301, PR333, PR328, PR325, PR322, PL300	X00
4	57	Vcorecapacitor reduce	2013/2/7	Power	Vcore output capacitor reduce	NC: PC371 ,PC386, PC370 ,PC382,PC383	X00
5	58	Charger	2013/2/18	Power	Reserve H_PROCHOT# delay time fine tune by soft ware	Add "MODULE_BATT_PRES#" and PR454(Cancel 3/19)	X00
6	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 240K to 100K: PR503, PR528, PR544, PR565	X00
7	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 47K to 240K: PR501, PR524, PR535, PR540	X00
8	59	P59-PWR_Selector	2013/2/26	Power	SUT will unexpected shut down if un-docking during S0/S3	Add: PQ528, PR566	X00
9	51	*PBAT_PRES# ESD fail	2013/3/4	Power	ESD PD1 fail, even connect 3.3V to VBUS pin	Change PD1 to PD1, PD2(TVNST52302AB0)	X00
10	59	P59-PWR_Selector	2013/3/6	Power	SB903380020 FDN338P derating fail	PQ500, PQ517,PQ520,PQ522,PQ526 change to SB000007900, PQ1change to SB000007900	X00
11	51	PC5 down size	2013/3/12	Power	PC5 down size	Change PC5 from 0805 to 0603 size	X00
12	51,59	AC_DIS# net change	2013/3/12	Power	AC_DIS# should high enable, not low enable	AC_DIS# change to AC_DIS	X00
13		EMC open issue	2013/3/18	Power	Add parts for EMI	PR606,PC615, PR632, PC628, PR706, PC705, PR324, PC307	X00
14	60, 62	PU600, PU601 VCC	2013/3/19	Power	DIS S3 power consumption voer 200mW	Add PR630 PR711, PR710 for reserve +5V_RUN	X00
15	61	Change DGPU output cap	2013/3/19	Power	For thermal issue change DGPU power output cap.-14"	Change PC683,PC684	X00
16	62	GPU DDR change to 1.35V	2013/3/19	Power	Change VDDR output voltage from 1.5V to 1.35V	Change PR707 from 11.5K to 9.1K	X00
17	54	+1.05V dynamic load test	2013/3/19	Power	+1.05V dynamic load over spec	Change PL150 from 1uH to 0.68uH	X00
18	58	Change output chock	2013/3/20	Power	Same as 14" for height limit	Charger output choke change to 2.2uH	X00
19	60	0 ohm resistor	2013/3/21	Power	0 ohm 1% vender is not correct in ISPD	Change PR621 0ohm from 1% to 5%	X00
20	54	1.05V dynamic over spec	2013/3/21	Power	1.05V dynamic over spec	Change PL150 from 1uH to 0.68uH	X00
21	59	Modify for Peak power	2013/3/21	Power	Modify schematic	PQ529, PQ518, PR527 and PR567	X00
22	NA	Reserve	Reserve	Power	Reserve	Reserve	X01
23	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	59	14* 組裝問題	2013/5/10	Power	PD512 太靠邊板	Move location	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	14" Vcore find tune	2013/5/29	Power	14" Vcore find tune for LL and DIMON	PR328=2.4K->2.1K; PR333=30K->49.9K; PR301=390K->348K	X02
2	NA	Reserve	Reserve	Power	Reserve	Reserve	X02
3	58	EMI solution	2013/5/31	EMI	EMI: 200-225MHz boardband	Populate bead 120 ohm on PJP100 and PL301, populate 0.1uF on pc302 and pc700, 2200pF on pc701.	X02
4	58	EMI solution	2013/5/31	EMI	EMI: 200-225MHz boardband	PC419 add parallel PC441:2200pF and PC440: 0.1uF	X02
5	62	Thermal de-ratgin issue	2013/6/10	Power	MLCC are exceeded thermal derating criteria	Change to X6S/X7R: PC600, PC601, PC604, PC605, PC674, PC302, PC304,PC311,PC312,PC313,PC314	X02
6	59	Change part number	2013/6/6	Power	Part number -N0 is for other customer	PC505 SE043474KN0 change to SE043474K80	X02
7	NA	14" NPI report(4/19)	2013/6/6	Power	Co-lay need select 1 component	Del NC: PJP300, PL600, PJP1, PC66, PC707, PJP51,PJP400	X02
8		Selector	2013/5/30	Power	For 3V/5V volgate level, change VDS rating from 30V to 20V	PQ1, PQ518 change to 20V rating DMG2301U-7_SOT23-3	X02
9	62	14" DGPU DDR	2013/6/7	Power	Output capacitor PC709 not in PSL	Change to NCC: SF0000003100	X02
XB							
1		Thermal de-ratgin issue	2013/7/10	Power	According QAD test result change MLCC back to X5R	PC674, PC302, PC304,PC311,PC312,PC313,PC314	X03
2		Change 0 ohm to short pad	2013/7/10	Power	Reduce part count	Except: PR321 and PR621	X03
3		Thermal de-ratgin issue	2013/7/10	Power	MLCC are exceeded thermal derating criteria	VAW30 change to X6S/X7R: PC302, PC304, PC311, PC312, PC313, PC314	X03

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